

Shilpa Bhoj

Objective

A challenging full-time position in the field of digital hardware design and design automation tool development.

Education

- **Ph.D. candidate in Computer Engineering** Spring 2006 - present
University of Texas at Dallas (UT Dallas) Expected Graduation: Sept 2008
Advisor: **Dr. Dinesh K. Bhatia.** GPA - 4.0/4.0
- **M.S. in Computer Engineering** Fall 2004 - Fall 2005
University of Texas at Dallas (UT Dallas) GPA - 4.0/4.0
- **BE(Hons) in Computer Science & Engg.** 2000 - 2004
Birla Inst. of Technology and Sciences (BITS), Pilani, India (Dubai Campus) GPA - 10.0/10.0
Recipient of Chancellor's Gold Medal for Academic Excellence (Ranked #1 in graduating class)

Research

1. Thermal & Power aware architectures and CAD tools for programmable fabrics

- Designed and implemented a mesh based thermal model in MATLAB and C, for rapid temperature profiling of FPGAs. The model was used to develop a simulated annealing based temperature aware FPGA placement tool
- Developed estimation algorithms to determine pre-route interconnect generated capacitance, static and dynamic power distribution.
- Developed an adaptive thermal management system to respond to time varying thermal distribution across reconfigurable fabrics. Tasks involved development of a C based FPGA temperature and power simulator, layout generation in Cadence and simulation and extraction of SPICE netlists.

2. Network on Chip based systems

- Designed and implemented parts of an image processing SoC consisting of a UART Controller, Memory Unit, JPEG and Processor cores interconnected using a chip level packet switched network. The system was implemented in Verilog on the Xilinx Virtex II FPGA.

Work Experience

- **Summer Intern** June - August 2007
Qualcomm, Inc. (Corporate R & D), San Diego, CA
Designed and implemented digital hardware blocks for a 4G Long Term Evolution (LTE) emulation platform. The functional blocks were designed to bridge the system processor with a 10 Gigabit Ethernet IP core. Primary tasks of the blocks included protocol conversion, data reorganization, handshake signal generation and data rate matching. The blocks were implemented in VHDL in the Altera Quartus design environment and extensively verified using VERA.
- **Teaching Assistant** Fall 2004 - Present
Electrical Engineering and Computer Science, University of Texas at Dallas
Courses Taught: Digital Circuits, Electronic Circuits, Electrical Network Analysis, Signals & Systems, Micro-processor Design Project, Control Systems
Work included supervising lab sessions and office hours; preparing and grading homework, midterms and quizzes.

Publications

1. Shilpa Bhoj, **Thermal Aware FPGA Architectures and CAD**, PhD Forum, *IEEE International Conference in Field Programmable Logic and Applications (FPL)*, Germany, 2008.
2. Shilpa Bhoj and Dinesh Bhatia, **A Dynamic Temperature Control Simulation System for FPGAs**, *IEEE International Conference in Field Programmable Logic and Applications (FPL)*, Germany, 2008.
3. Shilpa Bhoj and Dinesh Bhatia, **Early Stage FPGA Interconnect Leakage Power Estimation**, submitted to *IEEE International Conference on Computer Design (ICCD)*, Lake Tahoe, 2008.

4. Shilpa Bhoj and Dinesh Bhatia, **Pre-Route Interconnect Capacitance and Power Estimation in FPGAs**, *IEEE International Conference in Field Programmable Logic and Applications (FPL)*, Netherlands, August 2007.
5. Shilpa Bhoj and Dinesh Bhatia, **Thermal modeling and Temperature Driven Placement for FPGAs**, *IEEE International Symposium on Circuits and Systems (ISCAS)*, New Orleans, May 2007.
6. Shilpa Bhoj and Dinesh Bhatia, **Thermal Aware Placement in FPGAs**, to be submitted to *ACM Transactions on Reconfigurable Technology and Systems*.
7. Shilpa Bhoj and Dinesh Bhatia, **Adaptive Thermal Management in Reconfigurable Systems**, to be submitted to *ScienceDirect Journal of Embedded Hardware Design (MICPRO)*.
8. S. Singh, Shilpa Bhoj, D. Balasubramanian, T. Nagda, D. Bhatia, P. Balsara, **Network interface for NoC based architectures**, *Intl Journal of Electronics*, Volume 94, Issue 5, 2007.
9. S. Singh, Shilpa Bhoj, D. Balasubramanian, T. Nagda, D. Bhatia, P. Balsara, **Generic Network Interface for Plug and Play NoC based architectures**, *Lecture Notes in Computer Science, Vol 3985, Reconfigurable Computing: Architectures and Applications*, pp 287 - 298, 2006.

Relevant Graduate Courses

- VLSI Design, Design Automation of VLSI systems (CAD Algorithms), VHDL Modeling, Microprocessors, Design and Analysis of Computer Algorithms, Computer Architecture, Digital Signal Processing

Projects

1. VLSI Design

- Full custom ASIC implementation of rectangular to polar coordinate converter using the CORDIC algorithm. Cadence Virtuoso Editor used for schematic development and MAGIC v7.1 for layout. Simulation and analysis of implementation done in SPICE, IRSIM and SIMG.
- Design and Implementation of Simulated Annealing based CAD tool for circuit bipartitioning. Tool was implemented in C and tested on ISPD'98 suite of benchmark circuits.

2. Microcontrollers and Reconfigurable Systems

- Implementation of FPGA based CIDR forwarding engine for IPv4 using Altera Quartus Design flow. System implemented using NIOS II soft core programmed in C interfaced with a custom RTL based on chip lookup unit.
- Implementation of ATM cell forwarding engine using 8051 Microcontroller. Functionality included cell transfer using UART interface, lookup and header processing.
- Design and implementation of a UART Controller in VHDL/Verilog on Spartan 2 FPGA.

3. Computer Architecture and Operating Systems

- Implementation and analysis of Level 3 cache using the SimpleScalar tool.
- Implementation of Asynchronous check pointing and process termination algorithm.

4. Digital Signal Processing

- Design and implementation of Linear phase Window based FIR filters in MATLAB.

Technical Skills

- Languages: C/C++, VHDL/Verilog (RTL Coding & Testing), VERA, PERL, MATLAB
- Design Tools: Xilinx ISE Suite, Altera Quartus Platform & NIOS Kit, Cadence Virtuoso Editor, Leonardo Spectrum, MAGIC
- Simulators & Analysis tools: SimpleScalar, ModelSim, SPICE, IRSIM, DRC, LVS, VPR
- Assembly Level Programming: 80x86, 8051
- Operating Systems: UNIX, LINUX, Windows

References available upon request