Eric M. Vogel
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The University of Texas at Dallas
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Experience:

Associate Professor, The University of Texas at Dallas, Dept. of Electrical Engineering, ***8/06-present***

- Pursuing a dynamic and cross-disciplinary research program exploring devices, materials, and processes for extending, replacing and complementing CMOS including finFETs, non-silicon MOS, and neuro-inspired computing.
- Currently supervising a research group consisting of 1 post-doctoral research associate, 5 graduate students and 1 undergraduate student.

Group Leader, CMOS and Novel Devices Group, National Institute of Standards and Technology (NIST), ***10/01–5/06***

- Responsible for technical output, performance, solvency, personnel, and planning for the CMOS and Novel Devices group (CND) consisting of approximately 15 staff and associates. The CND group conducts experimental and modeling research related to the measurement and standards infrastructure for CMOS and beyond devices, and their constituent materials as required by the semiconductor industry. This includes Metal-Oxide-Semiconductor (MOS) device characterization and reliability, molecular electronics, silicon nanowires, organic electronics, spectroscopic ellipsometry, scanning capacitance microscopy, and nanofabrication.
- Approximately 1/3 of the CND group budget comes from external and internal competitive sources including International Sematech, DARPA, JPL, NIST Advanced Technology Program, and the NIST Competence Program.
- Supervised research of numerous post-doctoral researchers and graduate students.
- Chair of the 2002 NIST Research Advisory Committee that advises and makes recommendations to the NIST Director on scientific issues, concerns, and opportunities.

Director, NIST AML (Advanced Measurement Laboratory) Nanofab, ***2/03 – 1/06***

- Founding Director of the NIST AML Nanofab which opened in the summer of 2005 and provides researchers at NIST working on a variety of semiconductor and other nanotechnology research the ability to fabricate prototypical nanoscale test structures, measurement instruments, standard reference materials, and electronic devices. The NF consists of 1000 m^2 of Class 100 clean room space.
- Developed the vision, obtained operating funds, led a cross-laboratory strategic advisory committee, supervise Nanofab staff, and directed the fit-up and start-up process. Presented

over 40 overview talks describing the facility to numerous external organizations including NSF, NIH, DARPA, NSA, Defense Dept., and Congressional Staff.

Researcher, NIST, Semiconductor Electronics Division, ***6/98 – present***

- Performed a wide variety of experimental and modeling research on MOS devices, gate dielectric reliability physics, and nanodevices.
- Collaborated with numerous universities and companies including Univ. of Maryland, North Carolina State Univ., IBM and SEMATECH.

Research Assistant, North Carolina State University, ***6/94 – 6/98***

- Performed Ph.D. research on aspects related to characterization, modeling, fabrication, and development of rapid thermal chemical vapor deposited oxynitride dielectrics for use as a gate insulator in advanced MOS devices. Advisor: Dr. J. J. Wortman, ECE. Co-taught a graduate level physical electronics class in the electrical engineering department.

Competitive Funding:

The University of Texas at Dallas (8/06 – present)

- 2007, Nanoelectronics Research Initiative (NRI) SouthWest Academy for Nanoelectronics (SWAN), Nanoscale Characterization Task, $300k for 3 years (for UTD), Eric M. Vogel (PI-UTD), Moon Kim, Bruce Gnade. SWAN is an NRI center of 5 universities led by Sanjay Banerjee of UT-Austin.
- 2006, National Institute of Standards and Technology, "Metrology for Extreme CMOS Devices", $345k for 3 years, Eric M. Vogel (PI).

National Institute of Standards and Technology (5/98 – 5/06)

- 2005, SEMATECH, "Methodology for Measuring Work Functions and Band Offsets of the High-N/Metal Gate Electrode Stack, and Combinatorial Determination of Optimal Metal Gate Electrodes**",** $250k/1 year, Eric M. Vogel, Martin Green, John Suehle
- 2005 SEMATECH, "FeoL-BeoL Metrology: Development of Backside FTIR for the High-k/Metal Gate Stack", $50k/1 year, Eric M. Vogel, Christina Hacker, Anne Chaka, Emily Jarvis
- 2004, DARPA MoleApps, "Development and Validation of Molecular Electronics Test Structures", $1M/5 years, Roger Van Zee, Curt A. Richter, James D. Batteas, Michael J. Tarlov, Eric M. Vogel
- 2004, NIST Competence Program, "Metrology to Enable the Realization of Organic Electronics", $4M/5 years, Eric Lin, Curt Richter, Dean DeLongchamp, Jan Obrzut, Wen-li Wu, Daniel Fischer, Eric Vogel, Lee Richter
- 2004, SEMATECH, "Gate Dielectric Metrology: The Use of Charge Pumping for Measuring Electrically Active Defects in High-k Gate Dielectrics", $50k/1 year, Eric M. Vogel
- 2003, SEMATECH, "Gate Dielectric Metrology: C-V Measurements of Oxide Thickness", $50k/1 year, Eric M. Vogel
- 2002, NIST Advanced Technology Intramural Program, "The Missing Plateau: Confined Silicon Devices for ULSI Nanotechnology", $1.3M/3 years, Eric M. Vogel, Neil Zimmerman, John Bonevich
- 2002, SEMATECH, "Gate Dielectric Metrology: Electrical Characterization of Advanced Gate Dielectrics", $50k/1 year, Eric M. Vogel

- 1999, NIST Standard Reference Database Program, “Alternate Dielectrics for Silicon”, $195k/3 years, Eric M. Vogel

Education:

- Ph. D. in Electrical Engineering (8/98) - North Carolina State University
- M. S. in Electrical Engineering (5/96) - North Carolina State University
- B. S. in Electrical Engineering (5/94) - Pennsylvania State University

Other University Memberships:

- Adjunct Faculty Member North Carolina State University, faculty committee member of Chad Weintraub (Ph.D., August, 2000) and Heather Lazar (Ph. D., May, 2005)
- Special Faculty Member University of Maryland, Research Advisor of Da-wei Heh (Ph. D., May, 2005)

Industry Committees:

- International Technology Roadmap for Semiconductors, Emerging Research Materials Working Group, 3/04 - present
- International Technology Roadmap for Semiconductors, Front-End Processes Technical Working Group, 5/00 – 3/04
- SEMATECH Reliability Engineering Working Group, 11/98 – 11/01
- SEMATECH Gate Stack Engineering Working Group, 11/98 – 11/01

Conference Committees:

- IEEE International Reliability Physics Symposium Dielectrics Program Committee, 7/06 – present
- American Physical Society, Spring 2007 Meeting, Organizer of FIAP Focus Session on Emerging Research Devices and Materials for the Microelectronics Industry
- Workshop on Dielectrics in Microelectronics Program Committee, 11/02 – present
- IEEE Semiconductor Interface Specialists Conference, Executive Committee (2003 Arrangements Chair, 2004 Technical Chair, 2005 General Chair, 2006 Ex-Officio Chair)
- IEEE Semiconductor Interface Specialists Conference Program Committee, 1/00 – 1/03
- IEEE 2001 International Reliability Physics Symposium Dielectrics Program *Co-chair*
- IEEE International Reliability Physics Symposium Dielectrics Program Committee, 10/00 – 9/03
- IEEE Integrated Reliability Workshop Technical Program Committee, 5/01 – 9/03
- Co-organizer MRS Workshop on High-N Gate Dielectrics, June 1-2, 2000

Society Memberships:

- Institute of Electrical and Electronics Engineers (Senior Member), Materials Research Society, American Physical Society

Book Chapters:

3. C. R. Cleavelin, L. Columbo, H. Niimi, S. Pas, and E. M. Vogel, "Oxidation and Gate Dielectrics" to appear in *Handbook of Semiconductor Manufacturing Technology, vol. 2,* Y. Nishi and R. Doering, Editors, CRC Press (2007)

2. E. M. Vogel, and V. Misra, 'MOS Device Characterization,' in *Handbook of Silicon Semiconductor Metrology,* Marcel-Dekker, ed. A. C. Diebold, pp. 59-96, 2001.

1. C. R. Cleavelin, S. Pas, E. M. Vogel, and J. J. Wortman, 'Oxidation,' in *Handbook of Semiconductor Manufacturing Technology*, CRC Press, ed. Y. Nishi, and R. Doering, 2000.

Tutorials:

5. E. M. Vogel, "Electrical and Reliability Characterization of Advanced MOS Devices," 2-day Tutorial, Organized by Semyzen, Singapore, July 23-24, 2007.

4. E. M. Vogel, "Electrical Characterization of MOS Devices with Advanced Gate Stacks," Tutorial, 2005 MIGAS International School on Advanced Microelectronics, Physical and Electrical Characterization of Materials and Devices for Silicon Nanoelectronics, (http://www.migas.inpg.fr/), Grenoble, France, June 11-17, 2005.

3. E. M. Vogel, "Characterization, Physical Modeling, and Assessment of Gate Oxide Reliability," Tutorial, 2002 IEEE International Reliability Physics Symposium, Dallas, TX, April 7, 2002.

2. E. M. Vogel, "Ultra-thin Gate Oxide Reliability: Past and Present Trends in Characterization, Physical Modeling, and Assessment," Tutorial, 2001 IEEE Integrated Reliability Workshop, Lake Tahoe, CA, Oct. 15, 2001.

1. J. S. Suehle and E. M. Vogel, "Thin Gate Oxide Reliability," Tutorial, International Reliability Physics Symposium, Apr. 10, 2000.

Journal Publications (2 Invited*):

44. N. V. Nguyen, H. D. Xiong, J. S. Suehle, O. Kirillov, E. M. Vogel, P. Majhi and H.-C. Wen "Internal Photoemission Spectroscopy of [TaN/TaSiN] and [TaN/TaCN] Metal Stacks On SiO_2 and [HfO_2 / SiO_2] Dielectric Stack," submitted to *Appl. Phys. Lett.*

43. D. Heh, C. D. Young, G. A. Brown, P. Y. Hung, A. Diebold, E. M. Vogel, J. B. Bernstein, and G. Bersuker, "Spatial Distributions of Trapping Centers in HfO_2/SiO_2 Gate Stack," *IEEE Transactions on Electron Devices*, vol. 54, pp. 1338-1345, 2007.

42. Q. Li, S.-M. Koo, C. A. Richter, M. D. Edelstein, J. E. Bonevich, J. J. Kopanski, J. S. Suehle, and E. M. Vogel, "Precise alignment of single nanowires and fabrication of nanoelectromechanical switch and other test structures," *IEEE Transactions on Nanotechnology*, vol. 6, pp. 256-263, 2007.

*41. E. M. Vogel, "Technology and metrology of new electronic materials and devices," *Nature Nanotechnology*, vol. 2, pp. 25-32, 2007.

*40. C. M. Garner, and E. M. Vogel, "Metrology Challenges for Emerging Research Devices and Materials," *IEEE Transactions on Semiconductor Manufacturing*, vol. 19, pp. 397-403, 2006.

39. K.-S. Chang, M. Green, J. Suehle, E. Vogel, H. Xiong, J. Hattrick-Simpers, I. Takeuchi, O. Famodu, K. Ohmori, P. Ahmet, T. Chikyow, P. Majhi, B.-H. Lee, and M. Gardner, "Combinatorial Study of Ni-Ti-Pt Ternary Metal Gate Electrodes on HfO_2 for the Advanced Gate Stack," *Applied Physics Letters*, vol. 89, art no. 142108, 2006.

38. C. A. Richter, C. A. Hacker, L. J. Richter, O. A. Kirillov, J. S. Suehle, and E. M. Vogel, "Interface Characterization of Molecular-Monolayer/SiO_2 Based Molecular Junctions," *Solid-State Electronics*, vol. 50, pp. 1088-1096, 2006.

37. D. Heh, E. M. Vogel, J. B. Bernstein, C. D. Young, G. A. Brown, P. Y. Hung, and A. Diebold, G. Bersuker, "Spatial Distributions of Trapping Centers in HfO_2/SiO_2 Gate Stacks," *Applied Physics Letters*, vol. 88, art no. 152907, 2006.

36. S.-E. Park, N. V. Nguyen, J. J. Kopanski, J. S. Suehle, and E. M. Vogel, "Comparison of scanning capacitance microscopy and scanning Kelvin probe microscopy in determining two-dimensional doping profiles of Si homostructures," *Journal of Vacuum Science and Technology B*, vol. 24, pp. 404-407, 2006.

35. J. Ehrstein, C. Richter, D. Chandler-Horowitz, E. Vogel, C. Young, S. Shah, D. Maher, B. Foran, P. Y. Hung, and A. Diebold, "A Comparison of Thickness Values for Very Thin SiO_2 Films by Using Ellipsometric, Capacitance-Voltage, and HRTEM Measurements," *Journal of the Electrochemical Society*, vol. 153, pp. F12-F19, 2006.

34. S.-M. Koo, Q. Li, M. D. Edelstein, C. A. Richter, and E. M. Vogel, "Enhanced Channel Modulation in Dual-Gated Silicon Nanowire Transistors", *NanoLetters*, vol. 5, pp. 2519-2523, 2005.

33. S.-M. Koo, M. D. Edelstein, Q. Li, C. A. Richter, and E. M. Vogel, “Silicon nanowires as enhancement-mode Schottky-barrier field-effect transistors,” *Nanotechnology*, vol. 16, pp. 1482-1485, 2005.

32. G. K. Ramachandran, M. D. Edelstein, D. L. Blackburn, J. S. Suehle, E. M. Vogel, and C. A. Richter, “Nanometre gaps in gold wires are formed by thermal migration,” *Nanotechnology*, vol. 16, pp. 1294-1299, 2005.

31. J.-P. Han, S. M. Koo, E. M. Vogel, E. P. Gusev, C. D'Emic, C. A. Richter, and J. S. Suehle, ‘Reverse Short Channel Effects in High-k gated nMOSFETs,’ *Microelectronics Reliability*, vol. 45, pp. 783-785, 2005.

30. S.-M. Koo, A. Fujiwara, J.-P. Han, E. M. Vogel, C. A. Richter, and J. E. Bonevich, “High Inversion Current in Silicon Nanowire Field Effect Transistors,” *NanoLetters*, vol. 4, pp. 2197-2201, 2004.

29. N. V. Nguyen, J. E. Maslar, Jin-Yong Kim, Jin-Ping Han, Jin-Won Park, D. Chandler-Horowitz, and E. M. Vogel, “Crystalline Quality of Silicon-On-Insulator Characterized by Spectroscopic Ellipsometry and Raman Spectroscopy,” *Applied Physics Letters*, vol. 85, pp. 2765-2767, 2004.

28. J.-P. Han, S.-M. Koo, C. A. Richter, and E. M. Vogel, “Influence of buffer layer thickness on memory effects of $SrBi_2Ta_2O_9$/SiN/Si structures”, *Applied Physics Letters*, vol. 85, pp. 1439-1441, 2004.

27. C. A. Richter, C. Hacker, L. J. Richter, E. M. Vogel, "Molecular Devices Formed by Direct Monolayer Attachment to Silicon", *Solid-State Electronics*, vol. 48, pp. 1747-1752, 2004.

26. J.-P. Han, E. M. Vogel, E. P. Gusev, C. D'Emic, C. A. Richter, D. W. Heh, and J. S. Suehle, "Asymmetric Energy Distribution of Interface Traps in n- and p-MOSFETs with HfO2 Gate Dielectric on Ultrathin SiON Buffer Layer," *IEEE Electron Device Letters*, vol. 25, pp. 126-128, 2004.

25. E. M. Vogel, C. A. Richter, and B. G. Rennex, ‘A capacitance-voltage model for polysilicon-gated MOS devices including substrate quantization effects based on modification of the total semiconductor charge,’ *Solid-State Electronics*, vol. 47, pp. 1589-1596, 2003.

24. D.-W. Heh, E. M. Vogel, and J. B. Bernstein, ‘Impact of Substrate Hot Hole Injection on Ultra-thin Silicon Dioxide Breakdown,’ *Applied Physics Letters*, vol. 82, pp. 3242-3244, 2003.

23. E. M. Vogel, D.-W. Heh, and J. B. Bernstein, ‘Impact of the Trapping of Anode Hot Holes on Silicon Dioxide Breakdown,’ *IEEE Electron Device Letters*, vol. 23, pp. 667-669, 2002.

22. E. M. Vogel, D. Heh, and J. B. Bernstein, ‘Interaction between low energy electrons and defects created by hot holes in ultra-thin silicon dioxide,’ *Applied Physics Letters*, vol. 80, pp. 3343-3345, 2002.

21. J. S. Suehle, E. M. Vogel, P. Roitman, J. F. Conley, Jr., A. H. Johnston, B. Wang, J. B. Bernstein, and C. E. Weintraub, 'Observation of Latent Reliability Degradation in Ultra-Thin Oxides After Heavy-Ion Irradiation,' *Applied Physics Letters*, vol. 80, pp. 1282-1284, 2002.

20. J. F. Conley, Jr., J. S. Suehle, A. H. Johnston, B. Wang, T. Miyahara, E. M. Vogel, and J. B. Bernstein, 'Heavy Ion Induced Soft Breakdown of Thin Gate Oxides,' *IEEE Transactions on Nuclear Science*, vol. 48, pp. 1913-1916, 2001.

19. C. E. Weintraub, E. M. Vogel, N. Yang, V. Misra, J. J. Wortman, J. J. Ganem, and P. Masson, 'Application of Low Frequency Charge Pumping on Thin Stacked Dielectrics,' *IEEE Transactions on Electron Devices*, vol. 48, pp. 2754-2762, 2001.

18. E. M. Vogel, M. D. Edelstein, and J. S. Suehle, 'Reliability of Ultra-thin Silicon Dioxide Under Substrate Hot-electron, Substrate Hot-hole, and Tunneling Stress,' *Microelectronic Engineering*, vol. 59, pp. 73-83, 2001.

17. E. M. Vogel, M. D. Edelstein, and J. S. Suehle, 'Defect generation and breakdown of ultra-thin silicon dioxide induced by substrate hot-hole injection,' *Journal of Applied Physics*, vol. 90, pp. 2338-2346, 2001.

16. B.Wang, J. S. Suehle, E. M. Vogel, and J. B. Bernstein, 'Time-Dependent Breakdown of Ultra-Thin SiO_2 Gate Dielectrics Under Pulsed Biased Stress,' *IEEE Electron Device Letters*, vol. 22, pp. 224-226, 2001.

15. C. A. Richter, A. R. Hefner, and E. M. Vogel, 'A Comparison of Quantum-Mechanical Capacitance-Voltage Simulators,' *IEEE Electron Device Letters*, vol. 22, pp. 35-37, 2001.

14. W. K. Henson, N. Yang, S. Kubicek, E. M. Vogel, J. J. Wortman, K. De Meyer, and A. Naem, 'Analysis of Leakage Currents and Power Consumption for CMOS Technology in the 100 nm Regime,' *IEEE Transactions on Electron Devices*, vol. 47, pp.1393-1400, 2000.

13. E. M. Vogel, J. S. Suehle, M. D. Edelstein, B. Wang, Y. Chen, and J. B. Bernstein, 'Reliability of Ultra-thin Silicon Dioxide Under Combined Substrate Hot Electron and Constant Voltage Tunneling Stress,' *IEEE Transactions on Electron Devices*, vol. 47, pp. 1183-1191, 2000.

12. E. M. Vogel, W. K. Henson, C. A. Richter, and J. S. Suehle, 'Limitations of Conductance to the Measurement of the Interface State Density of MOS Capacitors with Tunneling Gate Dielectrics,' *IEEE Transactions on Electron Devices*, vol. 47, pp. 601-608, 2000.

11. A. Shanware, H. Z. Massoud, E. Vogel, K. Henson, J. R. Hauser, and J. J. Wortman, 'Modeling the Trends in Valence-Band Electron Tunneling in NMOSFETs with Ultrathin SiO_2 and SiO_2/Ta_2O_5 Dielectrics with Oxide Scaling,' *Microelectronic Engineering*, vol. 48, pp. 295-298, 1999.

10. P. Masson, P. Morfouli, J. L. Autran, J. Brini, B. Balland, E. M. Vogel, and J. J. Wortman, 'Electrical Properties of Oxynitride Thin Films Using Noise and Charge Pumping Measurements,' *Journal of Non-Crystalline Solids*, vol. 245, pp. 54-58, 1999.

9. W. K. Henson, K. Z. Ahmed, E. M. Vogel, J. R. Hauser, J. J. Wortman, R. Dätta, M. Xu and D. Venables, 'Estimating Oxide Thickness of Tunnel Oxides Down to 1.4 nm Using Conventional Capacitance-Voltage Measurements on MOS Capacitors,' *IEEE Electron Device Letters*, vol. 20, pp. 179-181, 1999.

8. V. Z-Q. Li, M. R. Mirabedini, E. Vogel, K. Henson, D. Batchelor, J. J. Wortman, and R. T. Kuehn, 'Effects of Si Source Gases (SiH_4 and Si_2H_6) on Polycrystalline-$Si_{1-x}Ge_x$ Deposited on Oxide by RTCVD,' *Electrochemical and Solid-State Letters*, vol. 1, pp. 153-155, 1998.

7. E. M. Vogel, K. Z. Ahmed, B. Hornung, W. K. Henson, P. K. McLarty, G. Lucovsky, J. R. Hauser, and J. J. Wortman, 'Modeled tunnel currents for high dielectric constant dielectrics,' *IEEE Transactions on Electron Devices*, vol. 45, pp.1350-1355, 1998.

6. P. Morfouli, G. Ghibaudo, E. M. Vogel, W. L. Hill, V. Misra, P. K. McLarty, and J. J. Wortman, 'Electrical and reliability properties of thin silicon oxynitride dielectrics formed by low pressure rapid thermal chemical vapor deposition' *Solid-State Electronics*, vol. 41, pp. 1051-1055, 1997.

5. P. Morfouli, G. Ghibaudo, T. Ouisse, E. Vogel, W. Hill, V. Misra, P. McLarty, and J. J. Wortman, 'Low-frequency noise characterization of n- and p- MOSFET's with ultrathin oxynitride gate films,' *IEEE Electron Device Letters*, vol. 17, pp. 395-397, 1996.

4. E. M. Vogel, W. L. Hill, V. Misra, P. K. McLarty, J. J. Wortman, J. R. Hauser, P. Morfouli, G. Ghibaudo, and T. Ouisse, 'Mobility behavior of n-channel and p-channel MOSFETs with oxynitride gate dielectrics formed by low-pressure rapid thermal chemical vapor deposition,' *IEEE Transactions on Electron Devices*, vol. 43, pp. 753-758, 1996.

3. V. Misra, W. K. Henson, E. M. Vogel, G. A. Hames, P. K. McLarty, J. R. Hauser, and J. J. Wortman, 'Electrical properties of composite gate oxides formed by rapid thermal processing,' *IEEE Transactions on Electron Devices*, vol. 43, pp. 636-646, 1996.

2. W. L. Hill, E. M. Vogel, V. Misra, P. K. McLarty, and J. J. Wortman, 'Low-pressure rapid thermal chemical vapor deposition of oxynitride gate dielectrics for n-channel and p-channel MOSFETs,' *IEEE Transactions on Electron Devices*, vol. 43, pp. 15-22, 1996.

1. W. L. Hill, E. M. Vogel, P. K. McLarty, V. Misra, J. J. Wortman, and V. Watt, 'N-channel and p-channel MOSFETs with gate dielectrics formed using low pressure rapid thermal chemical vapor deposition,' *Microelectronic Engineering*, vol. 28, pp. 269-272, 1995.

Conference Proceedings (6 Invited*):

*21. E. M. Vogel, A. M. Sonnet, and C. L. Hinkle, "Characterization of Electrically Active Interfacial Defects in High-κ Gate Dielectrics," submitted to *ECS Transactions*, 2007.

20. C. D. Young, S. Nadkarni, D. Heh, H. R. Harris, R. Choi, J. J. Peterson, J. H. Sim, S. A. Krishnan, J. Barnett, E. Vogel, B.H. Lee, P. Zeitzoff, G. A. Brown, and G. Bersuker, "Detection of Electron Trap Generation Due to Constant Voltage Stress on High-κ Gate Stacks," *IEEE International Reliability Physics Symposium Proceedings*, pp. 169-173, 2006.

19. C. D. Young, S. Nadkarni, D. Heh, H. R. Harris, R. Choi, J. J. Peterson, J. H. Sim, S. A. Krishnan, J. Barnett, E. Vogel, B.H. Lee, P. Zeitzoff, G. A. Brown, and G. Bersuker, "Detection of trap generation in high-kappa gate stacks," *IEEE Integrated Reliability Workshop Final Report*, pp. 79-83, 2005.

18. H. D. Xiong, N. V. Nguyen, J. J. Kopanski, J. S. Suehle, and E. M. Vogel, "Work function characterization of TaSiN and TaCN electrodes using CV, IV, IPE and SKPM," *ECS Transactions*, vol. 3, pp. 25-36, 2006.

*17. E. M. Vogel, D. Heh, "Characterization of electrically active defects in high-k gate dielectrics using charge pumping," in *NATO Advanced Research Workshop on Defects in Advanced High-k Dielectric Nanoelectronic Semiconductor Devices,* pp. 85-96, 2005.

*16. E. M. Vogel, "Physical Mechanisms of Ultra-thin Silicon Dioxide Degradation and Breakdown," Proceedings of the Electrochemical Society PV 2005-01, pp. 279-292, 2005

15. B. Zhu, J. S. Suehle, E. Vogel, and J. B. Bernstein, "The Contribution of HfO2 Bulk Oxide Traps to Dynamic NBTI in pMOSFETs," *IEEE International Reliability Physics Symposium Proceedings*, pp. 533-537, 2005.

*14. E. M. Vogel, "Metrology for Emerging Research Devices and Materials," in *Characterization and Metrology for ULSI Technology*, AIP Conference Proceedings, vol. 788, pp. 650-655, 2005.

13. N. V. Nguyen, J. E. Maslar, J.-Y. Kim, J.-P. Han, J.-W. Park, D. Chandler-Horowitz , and E. M. Vogel, "Characterization of Structural Quality of Bonded Silicon-on-Insulator Wafers by Spectroscopic Ellipsometry and Raman Spectroscopy," in *Materials Research Society Spring Meeting*, High-Mobility Group-IV Materials and Devices, pp. 127-132, 2004.

12. D. Heh, E. M. Vogel, and J. B. Bernstein, "New Insights into Threshold Voltage Shifts for Ultrathin Gate Oxides," *IEEE Integrated Reliability Workshop Final Report,* pp. 99-101, 2004.

11. J.-P. Han, E. M. Vogel, E.P. Gusev, C. D'Emic, C.A. Richter, D. W. Heh, J. Suehle, "Energy Distribution of Interface Traps in High-k Gated MOSFETs," *Digest of Technical Papers - Symposium on VLSI Technology*, pp. 161-162, 2003.

*10. E. M. Vogel, and G. A. Brown, “Challenges of Electrical Measurements of Advanced Gate Dielectrics in Metal-Oxide-Semiconductor Devices,” in *International Conference on Characterization and Metrology for ULSI Technology,* AIP Conference Proceedings, vol. 683, pp. 771-781, 2003.

9. J. Ehrstein, C. Richter, D. Chandler-Horowitz, E. Vogel, D. Ricks, C. Young, S. Spencer, S. Shah, D. Maher, B. Foran, A. Diebold, and P. Y. Hung, “Thickness evaluation for 2 nm SiO_2 films, a comparison of ellipsometric, capacitance-voltage and HRTEM measurements,” in *International Conference on Characterization and Metrology for ULSI Technology,* AIP Conference Proceedings, vol. 683, pp. 331-336, 2003.

8. D. Heh, J. B. Bernstein, E. M. Vogel, “Defect Generation in Ultra-thin Oxide Over Large Fluence Ranges,” *IEEE Integrated Reliability Workshop Final Report,* pp. , 2002.

7. B. Wang, J. S. Suehle, J. F. Conley, Jr., E. M. Vogel, C. E. Weintraub, A. H. Johnston, and J. B. Bernstein, “Latent Reliability Degradation of Ultra-Thin Oxides After Heavy Ion and γ –ray Irradiation,” *IEEE Integrated Reliability Workshop Final Report*, pp. 16-19, 2001.

6. B. Wang, J. S. Suehle, E. M. Vogel, and J. B. Bernstein, “The Effect of Stress Interruption and Pulsed Bias Stress on Ultra-thin Gate Dielectric Reliability,” *IEEE International Integrated Reliability Workshop Final Report*, pp. 74-79, 2000.

5. J. S. Suehle, E. M. Vogel, B. Wang, J. B. Bernstein, “Temperature Dependence of Soft Breakdown and Wear-Out in Sub 3 nm SiO_2 Films,” *IEEE International Reliability Physics Symposium Proceedings*, pp. 33-39, 2000.

4. A. Shanware, J. P. Shiely, H. Z. Massoud, E. Vogel, K. Henson, A. Srivastava, C. Osburn, J. R. Hauser, and J. J. Wortman, “Extraction of the Gate Oxide Thickness of N- and P-Channel MOSFETs Below 20 Å from the Substrate Current Resulting from Valence-Band Electron Tunneling,” *Technical Digest - International Electron Device Meeting*, pp. 815-819, 1999.

3. R. A. Allen, E. M. Vogel, L. W. Linholm, and M. W. Cresswell, “Sheet and Line Resistance of Patterned SOI Surface Film CD Reference Materials as a Function of Substrate Bias,” IEEE *International Conference on Microelectronic Test Structures*, pp. 51-55, 1999.

2. A. Srivastava, H. H. Heinisch, E. Vogel, C. Parker, C. M. Osburn, N. A. Masnari, J. J. Wortman, and J. R. Hauser, “Evaluation of 2.0 nm Grown and Deposited Dielectrics in 0.1 Pm PMOSFETs,” *Materials Research Society Symposium - Proceedings*, vol. 525, pp. 163-170, 1998.

*1. E. M. Vogel, J. J. Wortman, P. K. McLarty, V. H. C. Watt, and B. Kirkpatrick, “Silicon oxynitride films formed by rapid thermal chemical vapor deposition for VLSI applications,” *Proceedings of the Symposium on Silicon Nitride and Silicon Dioxide Thin Insulating Films*, vol. 97, pp. 394-407, 1997.

Conference and Other Presentations (23 Invited*):

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49. C. L. Hinkle, M. Milojevic, S. McDonnell, F. S. Aguirre-Tostado, A. M. Sonnet, R. M. Wallace, and E. M. Vogel, "GaAs Surface Modification by Arsenic Oxide Removal and Bond Conversion," submitted to 4th International Symposium on Advanced Gate Stack Technology, 2007.

*48. E. M. Vogel, "Metrology for Emerging Devices and Materials," American Materials Failure Analysis (AMFA) Workshop, Phoenix, AZ, April 20, 2007.

*47. E. M. Vogel, "Metrology for Beyond CMOS: Emerging Devices and Materials," 53rd American Vacuum Society International Symposium, Nano-Manufacturing Topical Conference, San Francisco, CA, Nov. 12-16, 2006.

*46. E. M. Vogel, "Technology and Metrology for Beyond CMOS," SEMATECH-SRC Topical Research Conference on Reliability, Austin, TX, Oct. 23, 2006.

45. Q. Li, S.-M. Koo, C. A. Richter, M. D. Edelstein, J. J. Kopanski, J. S. Suehle, and E. M. Vogel, "Precise Manipulation and Alignment of Single Nanowires for Device Fabrication," 2006 IEEE Silicon Nanoelectronics Workshop, Honolulu, HI, June 11-12, 2006.

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*42. E. M. Vogel, "Electrical Characterization of Defects in High-k Gate Dielectrics," International Semiconductor Device Research Symposium, Bethesda, MD, Dec. 7, 2005.

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39. M. Green and E. M. Vogel, "Method for Measuring the Barrier Height at the High-k/Metal Electrode Interface, and Combinatorial Determination of Optimal Metal Gate Electrodes," SEMATECH Advanced Gate Stack Engineering Working Group Biannual Meeting, Austin, TX, Feb. 14, 2005.

*38. E. M. Vogel and D. Heh, "Depth Profiles of Electrically Active Defects in High-k Gate Stacks Using Charge Pumping," SEMATECH Advanced Gate Stack Engineering Working Group Biannual Meeting, Austin, TX, Feb. 15, 2005.

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