

**Eric M. Vogel**

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**Educational History:**

Ph. D., 8/98, North Carolina State University - Raleigh NC, Electrical Engineering  
Thesis: "The Use of Rapid Thermal Chemical Vapor Deposited Oxynitrides for Advanced Gate Dielectrics," Advisor: Prof. Jim Wortman

M. S., 5/96, North Carolina State University - Raleigh NC, Electrical Engineering

B. S., 5/94, Pennsylvania State University – University Park PA, Electrical Engineering

**Employment History – principal positions since the Bachelor's degree:**

Associate Professor, 8/06-present, The University of Texas at Dallas, Department of Materials Science and Engineering, Department of Electrical Engineering, Richardson, TX

Founding Director of the NIST Nanofab, 2/03 – 1/06, NIST, Gaithersburg, MD

Leader of the CMOS and Novel Devices Group, 10/01–5/06, National Institute of Standards and Technology (NIST), Gaithersburg, MD

Researcher, 6/98 – 10/01, NIST, Gaithersburg, MD

Research Assistant, 6/94 – 6/98, North Carolina State University, Raleigh, NC

**Employment History – concurrent temporary or visiting appointments, consultanships:**

Adjunct Faculty Member, 8/99-5/05, North Carolina State University, Raleigh, NC

Special Faculty Member, 8/02-5/05, University of Maryland, College Park, MD

**Professional recognitions, honors, memberships, etc., (study, teaching, research, service):**

U.S. Dept. of Commerce Silver Medal, “For developing a vision, strategy, fit-up, fabrication processes, policies, protocols, and a safety program for the NIST AML Nanofab,” 2006, National Institute of Standards and Technology

Senior Member of the Institute of Electrical and Electronics Engineers

Member of the Materials Research Society

Member of the American Physical Society

**Books authored or co-authored:**

1. Oxidation and Gate Dielectrics  
C. R. Cleavelin, L. Columbo, H. Niimi, S. Pas, and E. M. Vogel,  
Book chapter in *Handbook of Semiconductor Manufacturing Technology*, 2<sup>nd</sup> edition,  
ed. Y. Nishi and R. Doering  
Taylor and Francis Group, 37 pages, 2007.
2. MOS Device Characterization  
E. M. Vogel, and V. Misra,  
Book chapter in *Handbook of Silicon Semiconductor Metrology*, ed. A. C. Diebold  
Marcel-Dekker, 37 pages, 2001.
3. Oxidation  
C. R. Cleavelin, S. Pas, E. M. Vogel, and J. J. Wortman,  
Book chapter in *Handbook of Semiconductor Manufacturing Technology*,  
ed. Y. Nishi and R. Doering,  
CRC Press, 22 pages, 2000.

**Articles in refereed journals (\*2 invited):**

1. Extraction of the Effective Mobility of In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSFETs  
C. L. Hinkle, A. M. Sonnet, R. A. Chapman, and E. M. Vogel  
Accepted *IEEE Electron Device Letters*
2. Half-cycle ALD reaction studies of Al<sub>2</sub>O<sub>3</sub> on (NH<sub>4</sub>)<sub>2</sub>S<sub>2</sub> passivated GaAs(100) surfaces  
M. Milojevic, C. L. Hinkle, F. S. Aguirre-Tostado, H. C. Kim, E. M. Vogel, J. Kim and R. M. Wallace  
*Applied Physics Letters*, 93, 252905 (2008). [Link](#)
3. Half-cycle atomic layer deposition reaction studies of Al<sub>2</sub>O<sub>3</sub> on In<sub>0.2</sub>Ga<sub>0.8</sub>As (100) surfaces  
M. Milojevic, F. S. Aguirre-Tostado, C. L. Hinkle, H. C. Kim, E. M. Vogel, J. Kim, and R. M. Wallace  
*Applied Physics Letters*, 93, 202902 (2008). [Link](#)
4. S passivation of GaAs and band bending reduction upon atomic layer deposition of HfO<sub>2</sub>/Al<sub>2</sub>O<sub>3</sub> nanolaminates  
F. S. Aguirre-Tostado, M. Milojevic, K. J. Choi, H. C. Kim, C. L. Hinkle, E. M. Vogel, J. Kim, T. Yang, Y. Xuan, P. D. Ye, and R. M. Wallace  
*Applied Physics Letters*, 93, 061907 (2008). [Link](#)
5. Smooth and uniform Al<sub>2</sub>O<sub>3</sub> dielectric layer deposited by atomic layer deposition for graphene-based nanoelectrics  
B. Lee, H.-C. Kim, M. Kim, R. M. Wallace, E. M. Vogel and J. Kim

- Applied Physics Letters*, 92, 203102 (2008). [Link](#)
6. Indium stability on InGaAs during atomic H surface cleaning  
F. S. Aguirre-Tostado, M. Milojevic, C. L. Hinkle, E. M. Vogel, R. M. Wallace, S. McDonnell, and G. J. Hughes  
*Applied Physics Letters*, 92, 171906 (2008). [Link](#)
  7. Impact of Semiconductor/Contact Metal Thickness Ratio on Organic Thin Film Transistor Performance  
S. Gowrisanker, Y. Ai, M. A. Quevedo-Lopez, H. Jia, H. N. Alshareef, E. Vogel, and B. Gnade  
*Applied Physics Letters*, 92, 153305 (2008). [Link](#)
  8. Performance enhancement of n-channel inversion type  $\text{In}_x\text{Ga}_{1-x}\text{As}$  metal-oxide-semiconductor field effect transistor using ex-situ deposited thin amorphous silicon layer  
A. M. Sonnet, C. L. Hinkle, M. N. Jivani, R. A. Chapman, G. P. Pollack, R. M. Wallace, and E. M. Vogel  
*Applied Physics Letters*, 93, 122109 (2008). [Link](#)
  9. Comparison of n-type and p-type GaAs oxide growth and its effects on frequency dispersion characteristics  
C. L. Hinkle, A. M. Sonnet, E. M. Vogel, M. Milojevic, F. S. Aguirre-Tostado, H. C. Kim, J. Kim, and R. M. Wallace  
*Applied Physics Letters*, 93, 113506 (2008). [Link](#)
  10. GaAs interfacial self-cleaning by atomic layer deposition  
C. L. Hinkle, A. Sonnet, E. M. Vogel, S. McDonnell, G. Hughes, M. Milojevic, B. Lee, F. Aguirre-Tostado, K.-J. Choi, H. Kim, J. Kim, and R. M. Wallace  
*Applied Physics Letters*, 92, 071901 (2008). [Link](#)
  11. Internal Photoemission Spectroscopy of [TaN/TaSiN] and [TaN/TaCN] Metal Stacks On  $\text{SiO}_2$  and [ $\text{HfO}_2 / \text{SiO}_2$ ] Dielectric Stack  
N. V. Nguyen, H. D. Xiong, J. S. Suehle, O. Kirillov, E. M. Vogel, P. Majhi and H.-C. Wen  
*Applied Physics Letters*, 92, 092907 (2008). [Link](#)
  12. Frequency dispersion reduction and bond conversion on n-type GaAs by in-situ surface oxide removal and passivation  
C. L. Hinkle, A. M. Sonnet, E. M. Vogel, S. McDonnell, M. Milojevic, B. Lee, F. S. Aguirre-Tostado, K. J. Choi, J. Kim, and R. M. Wallace  
*Applied Physics Letters*, 91, 163512 (2007). [Link](#)
  13. Spatial Distributions of Trapping Centers in  $\text{HfO}_2/\text{SiO}_2$  Gate Stack  
D. Heh, C. D. Young, G. A. Brown, P. Y. Hung, A. Diebold, E. M. Vogel, J. B. Bernstein, and G. Bersuker  
*IEEE Transactions on Electron Devices*, 54, 1338-1345 (2007). [Link](#)

14. Precise alignment of single nanowires and fabrication of nanoelectromechanical switch and other test structures  
Q. Li, S.-M. Koo, C. A. Richter, M. D. Edelstein, J. E. Bonevich, J. J. Kopanski, J. S. Suehle, and E. M. Vogel  
*IEEE Transactions on Nanotechnology*, 6, 256-263 (2007). [Link](#)
15. Technology and metrology of new electronic materials and devices  
E. M. Vogel  
*Nature Nanotechnology*, 2, 25-32 (2007). **\*invited.** [Link](#)
16. Three-dimensional simulation study of the improved on/off current ratio in silicon nanowire field-effect transistors  
C. Y. Choi, W. J. Cho, S. M. Koo, S. Kim, Q. Li, J. S. Suehle, C. A. Richter, and E. M. Vogel,  
*Journal of the Korean Physical Society*, 53, 1680-1684 (2007).
17. 14 MHz organic diodes fabricated using photolithographic processes  
Y. Ai, S. Gowrisanker, H. Jia, I. Trachtenberg, E. Vogel, R. M. Wallace, B. E. Gnade, R. Barnett, H. Stiegler, and H. Edwards  
*Applied Physics Letters*, 90, 262105 (2007). [Link](#)
18. Metrology Challenges for Emerging Research Devices and Materials  
C. M. Garner, and E. M. Vogel  
*IEEE Transactions on Semiconductor Manufacturing*, 19, 397-403 (2006). **\*invited** [Link](#)
19. Spatial Distributions of Trapping Centers in HfO<sub>2</sub>/SiO<sub>2</sub> Gate Stacks  
D. Heh, E. M. Vogel, J. B. Bernstein, C. D. Young, G. A. Brown, P. Y. Hung, A. Diebold, and G. Bersuker  
*Applied Physics Letters*, 88, 152907 (2006). [Link](#)
20. A Comparison of Thickness Values for Very Thin SiO<sub>2</sub> Films by Using Ellipsometric, Capacitance-Voltage, and HRTEM Measurements  
J. Ehrstein, C. Richter, D. Chandler-Horowitz, E. Vogel, C. Young, S. Shah, D. Maher, B. Foran, P. Y. Hung, and A. Diebold  
*Journal of the Electrochemical Society*, 153, F12-F19 (2006). [Link](#)
21. Comparison of scanning capacitance microscopy and scanning Kelvin probe microscopy in determining two-dimensional doping profiles of Si homostructures  
S.-E. Park, N. V. Nguyen, J. J. Kopanski, J. S. Suehle, and E. M. Vogel  
*Journal of Vacuum Science and Technology B*, 24, 404-407 (2006). [Link](#)
22. Combinatorial Study of Ni-Ti-Pt Ternary Metal Gate Electrodes on HfO<sub>2</sub> for the Advanced Gate Stack  
K.-S. Chang, M. Green, J. Suehle, E. Vogel, H. Xiong, J. Hattrick-Simpers, I. Takeuchi, O. Famodu, K. Ohmori, P. Ahmet, T. Chikyow, P. Majhi, B.-H. Lee, and M. Gardner  
*Applied Physics Letters*, 89, 142108 (2006). [Link](#)

23. Interface Characterization of Molecular-Monolayer/SiO<sub>2</sub> Based Molecular Junctions,  
C. A. Richter, C. A. Hacker, L. J. Richter, O. A. Kirillov, J. S. Suehle, and E. M. Vogel,  
*Solid-State Electronics*, 50, 1088-1096 (2006). [Link](#)
24. Enhanced Channel Modulation in Dual-Gated Silicon Nanowire Transistors  
S.-M. Koo, Q. Li, M. D. Edelstein, C. A. Richter, and E. M. Vogel  
*NanoLetters*, 5, 2519-2523 (2005). [Link](#)
25. Silicon nanowires as enhancement-mode Schottky-barrier field-effect transistors  
S.-M. Koo, M. D. Edelstein, Q. Li, C. A. Richter, and E. M. Vogel  
*Nanotechnology*, 16, 1482-1485 (2005). [Link](#)
26. Reverse Short Channel Effects in High-k gated nMOSFETs  
J.-P. Han, S. M. Koo, E. M. Vogel, E. P. Gusev, C. D'Emic, C. A. Richter, and J. S. Suehle  
*Microelectronics Reliability*, 45, 783-785 (2005). [Link](#)
27. Nanometre gaps in gold wires are formed by thermal migration  
G. K. Ramachandran, M. D. Edelstein, D. L. Blackburn, J. S. Suehle, E. M. Vogel, and C. A. Richter  
*Nanotechnology*, 16, 1294-1299 (2005). [Link](#)
28. High Inversion Current in Silicon Nanowire Field Effect Transistors  
S.-M. Koo, A. Fujiwara, J.-P. Han, E. M. Vogel, C. A. Richter, and J. E. Bonevich  
*NanoLetters*, 4, 2197-2201 (2004). [Link](#)
29. Influence of buffer layer thickness on memory effects of SrBi<sub>2</sub>Ta<sub>2</sub>O<sub>9</sub>/SiN/Si structures  
J.-P. Han, S.-M. Koo, C. A. Richter, and E. M. Vogel  
*Applied Physics Letters*, 85, 1439-1441 (2004). [Link](#)
30. Asymmetric Energy Distribution of Interface Traps in n- and p-MOSFETs with HfO<sub>2</sub> Gate Dielectric on Ultrathin SiON Buffer Layer  
J.-P. Han, E. M. Vogel, E. P. Gusev, C. D'Emic, C. A. Richter, D. W. Heh, and J. S. Suehle,  
*IEEE Electron Device Letters*, 25, 126-128 (2004). [Link](#)
31. Crystalline Quality of Silicon-On-Insulator Characterized by Spectroscopic Ellipsometry and Raman Spectroscopy  
N. V. Nguyen, J. E. Maslar, Jin-Yong Kim, Jin-Ping Han, Jin-Won Park, D. Chandler-Horowitz, and E. M. Vogel  
*Applied Physics Letters*, 85, 2765-2767 (2004). [Link](#)
32. Molecular Devices Formed by Direct Monolayer Attachment to Silicon  
C. A. Richter, C. Hacker, L. J. Richter, and E. M. Vogel  
*Solid-State Electronics*, vol. 48, 1747-1752 (2004). [Link](#)
33. A capacitance-voltage model for polysilicon-gated MOS devices including substrate quantization effects based on modification of the total semiconductor charge  
E. M. Vogel, C. A. Richter, and B. G. Rennex

- Solid-State Electronics*, 47, 1589-1596 (2003). [Link](#)
34. Impact of Substrate Hot Hole Injection on Ultra-thin Silicon Dioxide Breakdown  
D. Heh, E. M. Vogel, and J. B. Bernstein  
*Applied Physics Letters*, 82, 3242-3244 (2003). [Link](#)
35. Impact of the Trapping of Anode Hot Holes on Silicon Dioxide Breakdown  
E. M. Vogel, D.-W. Heh, and J. B. Bernstein  
*IEEE Electron Device Letters*, 23, 667-669 (2002). [Link](#)
36. Interaction between low energy electrons and defects created by hot holes in ultra-thin silicon dioxide  
E. M. Vogel, D. Heh, and J. B. Bernstein  
*Applied Physics Letters*, 80, 3343-3345 (2002). [Link](#)
37. Observation of Latent Reliability Degradation in Ultra-Thin Oxides After Heavy-Ion Irradiation  
J. S. Suehle, E. M. Vogel, P. Roitman, J. F. Conley, Jr., A. H. Johnston, B. Wang, J. B. Bernstein, and C. E. Weintraub  
*Applied Physics Letters*, 80, 1282-1284 (2002). [Link](#)
38. Application of Low Frequency Charge Pumping on Thin Stacked Dielectrics  
C. E. Weintraub, E. M. Vogel, N. Yang, V. Misra, J. J. Wortman, J. J. Ganem, and P. Masson  
*IEEE Transactions on Electron Devices*, 48, 2754-2762 (2001). [Link](#)
39. Time-Dependent Breakdown of Ultra-Thin SiO<sub>2</sub> Gate Dielectrics Under Pulsed Biased Stress  
B. Wang, J. S. Suehle, E. M. Vogel, and J. B. Bernstein  
*IEEE Electron Device Letters*, 22, 224-226 (2001). [Link](#)
40. A Comparison of Quantum-Mechanical Capacitance-Voltage Simulators  
C. A. Richter, A. R. Hefner, and E. M. Vogel  
*IEEE Electron Device Letters*, 22, 35-37 (2001). [Link](#)
41. Reliability of Ultra-thin Silicon Dioxide Under Substrate Hot-electron, Substrate Hot-hole, and Tunneling Stress  
E. M. Vogel, M. D. Edelstein, and J. S. Suehle  
*Microelectronic Engineering*, 59, 73-83 (2001). [Link](#)
42. Defect generation and breakdown of ultra-thin silicon dioxide induced by substrate hot-hole injection  
E. M. Vogel, M. D. Edelstein, and J. S. Suehle  
*Journal of Applied Physics*, 90, 2338-2346 (2001). [Link](#)
43. Heavy Ion Induced Soft Breakdown of Thin Gate Oxides  
J. F. Conley, Jr., J. S. Suehle, A. H. Johnston, B. Wang, T. Miyahara, E. M. Vogel, and J. B. Bernstein  
*IEEE Transactions on Nuclear Science*, 48, 1913-1916 (2001). [Link](#)

44. Reliability of Ultra-thin Silicon Dioxide Under Combined Substrate Hot Electron and Constant Voltage Tunneling Stress  
E. M. Vogel, J. S. Suehle, M. D. Edelstein, B. Wang, Y. Chen, and J. B. Bernstein  
*IEEE Transactions on Electron Devices*, 47, 1183-1191 (2000). [Link](#)
45. Limitations of Conductance to the Measurement of the Interface State Density of MOS Capacitors with Tunneling Gate Dielectrics  
E. M. Vogel, W. K. Henson, C. A. Richter, and J. S. Suehle,  
*IEEE Transactions on Electron Devices*, 47, 601-608 (2000). [Link](#)
46. Analysis of Leakage Currents and Power Consumption for CMOS Technology in the 100 nm Regime  
W. K. Henson, N. Yang, S. Kubicek, E. M. Vogel, J. J. Wortman, K. De Meyer, and A. Naem  
*IEEE Transactions on Electron Devices*, 47, 1393-1400 (2000). [Link](#)
47. Modeling the Trends in Valence-Band Electron Tunneling in NMOSFETs with Ultrathin SiO<sub>2</sub> and SiO<sub>2</sub>/Ta<sub>2</sub>O<sub>5</sub> Dielectrics with Oxide Scaling  
A. Shanware, H. Z. Massoud, E. Vogel, K. Henson, J. R. Hauser, and J. J. Wortman  
*Microelectronic Engineering*, 48, 295-298 (1999). [Link](#)
48. Electrical Properties of Oxynitride Thin Films Using Noise and Charge Pumping Measurements  
P. Masson, P. Morfouli, J. L. Autran, J. Brini, B. Balland, E. M. Vogel, and J. J. Wortman  
*Journal of Non-Crystalline Solids*, 245, 54-58 (1999). [Link](#)
49. Estimating Oxide Thickness of Tunnel Oxides Down to 1.4 nm Using Conventional Capacitance-Voltage Measurements on MOS Capacitors  
W. K. Henson, K. Z. Ahmed, E. M. Vogel, J. R. Hauser, J. J. Wortman, R. Datta, M. Xu and D. Venables  
*IEEE Electron Device Letters*, 20, 179-181 (1999). [Link](#)
50. Effects of Si Source Gases (SiH<sub>4</sub> and Si<sub>2</sub>H<sub>6</sub>) on Polycrystalline-Si<sub>1-x</sub>Ge<sub>x</sub> Deposited on Oxide by RTCVD  
V. Z-Q. Li, M. R. Mirabedini, E. Vogel, K. Henson, D. Batchelor, J. J. Wortman, and R. T. Kuehn  
*Electrochemical and Solid-State Letters*, 1, 153-155 (1998). [Link](#)
51. Modeled tunnel currents for high dielectric constant dielectrics  
E. M. Vogel, K. Z. Ahmed, B. Hornung, W. K. Henson, P. K. McLarty, G. Lucovsky, J. R. Hauser, and J. J. Wortman  
*IEEE Transactions on Electron Devices*, 45, 1350-1355 (1998). [Link](#)
52. Electrical and reliability properties of thin silicon oxynitride dielectrics formed by low pressure rapid thermal chemical vapor deposition

P. Morfouli, G. Ghibaudo, E. M. Vogel, W. L. Hill, V. Misra, P. K. McLarty, and J. J. Wortman  
*Solid-State Electronics*, 41, 1051-1055 (1997). [Link](#)

53. Low-frequency noise characterization of n- and p- MOSFET's with ultrathin oxynitride gate films  
P. Morfouli, G. Ghibaudo, T. Ouisse, E. Vogel, W. Hill, V. Misra, P. McLarty, and J. J. Wortman  
*IEEE Electron Device Letters*, 17, 395-397 (1996). [Link](#)
54. Mobility behavior of n-channel and p-channel MOSFETs with oxynitride gate dielectrics formed by low-pressure rapid thermal chemical vapor deposition  
E. M. Vogel, W. L. Hill, V. Misra, P. K. McLarty, J. J. Wortman, J. R. Hauser, P. Morfouli, G. Ghibaudo, and T. Ouisse  
*IEEE Transactions on Electron Devices*, 43, 753-758 (1996). [Link](#)
55. Electrical properties of composite gate oxides formed by rapid thermal processing  
V. Misra, W. K. Henson, E. M. Vogel, G. A. Hames, P. K. McLarty, J. R. Hauser, and J. J. Wortman  
*IEEE Transactions on Electron Devices*, 43, 636-646 (1996). [Link](#)
56. Low-pressure rapid thermal chemical vapor deposition of oxynitride gate dielectrics for n-channel and p-channel MOSFETs  
W. L. Hill, E. M. Vogel, V. Misra, P. K. McLarty, and J. J. Wortman,  
*IEEE Transactions on Electron Devices*, 43, 15-22 (1996). [Link](#)
57. N-channel and p-channel MOSFETs with gate dielectrics formed using low pressure rapid thermal chemical vapor deposition  
W. L. Hill, E. M. Vogel, P. K. McLarty, V. Misra, J. J. Wortman, and V. Watt  
*Microelectronic Engineering*, 28, 269-272 (1995). [Link](#)

**Articles appearing as chapters in edited volumes, self-mounted exhibitions, etc (\*6 invited):**

58. A gate dielectric last approach to integrate organic based devices on plastic substrates  
S. Gowrisanker, Y. Ai, M. A. Quevedo-Lopez, H. Jia, E. Vogel, and B. Gnade,  
*Proceedings of the Academic Track of the 2008 Flexible Electronics and Displays - Conference and Exhibition*, art. no. 4483882 (2008).
59. Characterization of Electrically Active Interfacial Defects in High- $\kappa$  Gate Dielectrics  
E. M. Vogel, A. M. Sonnet, and C. L. Hinkle,  
*ECS Transactions*, 11, 393 (2007). **\*invited** [Link](#)
60. Detection of Electron Trap Generation Due to Constant Voltage Stress on High- $\kappa$  Gate Stacks

- C. D. Young, S. Nadkarni, D. Heh, H. R. Harris, R. Choi, J. J. Peterson, J. H. Sim, S. A. Krishnan, J. Barnett, E. Vogel, B.H. Lee, P. Zeitzoff, G. A. Brown, and G. Bersuker  
*IEEE International Reliability Physics Symposium Proceedings*, 169-173 (2006). [Link](#)
61. Work function characterization of TaSiN and TaCN electrodes using CV, IV, IPE and SKPM  
H. D. Xiong, N. V. Nguyen, J. J. Kopanski, J. S. Suehle, and E. M. Vogel  
*ECS Transactions*, 3, 25-36 (2006). [Link](#)
62. Characterization of electrically active defects in high-k gate dielectrics using charge pumping  
E. M. Vogel and D. Heh  
*NATO Advanced Research Workshop on Defects in Advanced High-k Dielectric Nanoelectronic Semiconductor Devices*, 85-96 (2005). **\*invited**
63. Physical Mechanisms of Ultra-thin Silicon Dioxide Degradation and Breakdown  
E. M. Vogel  
*Proceedings of the Electrochemical Society*, 279-292 (2005). **\*invited** [Link](#)
64. Metrology for Emerging Research Devices and Materials  
E. M. Vogel  
*Characterization and Metrology for ULSI Technology, AIP Conference Proceedings*, 788, 650-655 (2005). **\*invited** [Link](#)
65. Detection of trap generation in high-kappa gate stacks  
C. D. Young, S. Nadkarni, D. Heh, H. R. Harris, R. Choi, J. J. Peterson, J. H. Sim, S. A. Krishnan, J. Barnett, E. Vogel, B.H. Lee, P. Zeitzoff, G. A. Brown, and G. Bersuker  
*IEEE Integrated Reliability Workshop Final Report*, 79-83 (2005). [Link](#)
66. The Contribution of HfO<sub>2</sub> Bulk Oxide Traps to Dynamic NBTI in pMOSFETs  
B. Zhu, J. S. Suehle, E. Vogel, and J. B. Bernstein  
*IEEE International Reliability Physics Symposium Proceedings*, 533-537 (2005). [Link](#)
67. New Insights into Threshold Voltage Shifts for Ultrathin Gate Oxides  
D. Heh, E. M. Vogel, and J. B. Bernstein  
*IEEE Integrated Reliability Workshop Final Report*, 99-101 (2004). [Link](#)
68. Characterization of Structural Quality of Bonded Silicon-on-Insulator Wafers by Spectroscopic Ellipsometry and Raman Spectroscopy  
N. V. Nguyen, J. E. Maslar, J.-Y. Kim, J.-P. Han, J.-W. Park, D. Chandler-Horowitz, and E. M. Vogel  
*MRS Symp. Proc., High-Mobility Group-IV Materials and Devices*, 127-132 (2004).
69. Energy Distribution of Interface Traps in High-k Gated MOSFETs  
J.-P. Han, E. M. Vogel, E. P. Gusev, C. D'Emic, C. A. Richter, D. Heh, and J. Suehle  
*Digest of Technical Papers - Symposium on VLSI Technology*, 161-162 (2003). [Link](#)

70. Challenges of Electrical Measurements of Advanced Gate Dielectrics in Metal-Oxide-Semiconductor Devices  
E. M. Vogel, and G. A. Brown  
*International Conference on Characterization and Metrology for ULSI Technology, AIP Conference Proceedings*, 683, 771-781 (2003). \*invited [Link](#)
71. Thickness evaluation for 2 nm SiO<sub>2</sub> films, a comparison of ellipsometric, capacitance-voltage and HRTEM measurements  
J. Ehrstein, C. Richter, D. Chandler-Horowitz, E. Vogel, D. Ricks, C. Young, S. Spencer, S. Shah, D. Maher, B. Foran, A. Diebold, and P. Y. Hung  
*International Conference on Characterization and Metrology for ULSI Technology, AIP Conference Proceedings*, 683, 331-336 (2003). [Link](#)
72. Defect Generation in Ultra-thin Oxide Over Large Fluence Ranges  
D. Heh, J. B. Bernstein, and E. M. Vogel,  
*IEEE Integrated Reliability Workshop Final Report* (2002). [Link](#)
73. Latent Reliability Degradation of Ultra-Thin Oxides After Heavy Ion and  $\gamma$  -ray Irradiation  
B. Wang, J. S. Suehle, J. F. Conley, Jr., E. M. Vogel, C. E. Weintraub, A. H. Johnston, and J. B. Bernstein  
*IEEE Integrated Reliability Workshop Final Report*, 16-19 (2001). [Link](#)
74. The Effect of Stress Interruption and Pulsed Bias Stress on Ultra-thin Gate Dielectric Reliability  
B. Wang, J. S. Suehle, E. M. Vogel, and J. B. Bernstein  
*IEEE International Integrated Reliability Workshop Final Report*, 74-79 (2000). [Link](#)
75. Temperature Dependence of Soft Breakdown and Wear-Out in Sub 3 nm SiO<sub>2</sub> Films  
J. S. Suehle, E. M. Vogel, B. Wang, and J. B. Bernstein  
*IEEE International Reliability Physics Symposium Proceedings*, 33-39 (2000). [Link](#)
76. Extraction of the Gate Oxide Thickness of N- and P-Channel MOSFETs Below 20 Å from the Substrate Current Resulting from Valence-Band Electron Tunneling  
A. Shanware, J. P. Shiely, H. Z. Massoud, E. Vogel, K. Henson, A. Srivastava, C. Osburn, J. R. Hauser, and J. J. Wortman  
*Technical Digest - International Electron Device Meeting*, 815-819 (1999). [Link](#)
77. Sheet and Line Resistance of Patterned SOI Surface Film CD Reference Materials as a Function of Substrate Bias  
R. A. Allen, E. M. Vogel, L. W. Linholm, and M. W. Cresswell  
*IEEE International Conference on Microelectronic Test Structures*, 51-55 (1999). [Link](#)
78. Evaluation of 2.0 nm Grown and Deposited Dielectrics in 0.1  $\mu$ m PMOSFETs  
A. Srivastava, H. H. Heinisch, E. Vogel, C. Parker, C. M. Osburn, N. A. Masnari, J. J. Wortman, and J. R. Hauser  
*Materials Research Society Symposium Proceedings*, 525, 163-170 (1998).

79. Silicon oxynitride films formed by rapid thermal chemical vapor deposition for VLSI applications  
E. M. Vogel, J. J. Wortman, P. K. McLarty, V. H. C. Watt, and B. Kirkpatrick  
*Proceedings of the Symposium on Silicon Nitride and Silicon Dioxide Thin Insulating Films*,  
97, 394-407 (1997). **\*invited**

**Invited or refereed talks/presentations to professional meetings and seminar or colloquia assemblies:**

*Tutorials (\*5 invited):*

1. Electrical and Reliability Characterization of Advanced MOS Devices  
E. M. Vogel  
Organized by Semyzen, Singapore, July 23-24, 2007. **\*invited**
2. Electrical Characterization of MOS Devices with Advanced Gate Stacks  
E. M. Vogel  
MIGAS International School on Advanced Microelectronics, Physical and Electrical Characterization of Materials and Devices for Silicon Nanoelectronics, (<http://www.migas.inpg.fr/>), Grenoble, France, June 11-17, 2005. **\*invited**
3. Characterization, Physical Modeling, and Assessment of Gate Oxide Reliability  
E. M. Vogel  
IEEE International Reliability Physics Symposium, Dallas, TX, April 7, 2002. **\*invited**
4. Ultra-thin Gate Oxide Reliability: Past and Present Trends in Characterization, Physical Modeling, and Assessment  
E. M. Vogel  
IEEE Integrated Reliability Workshop, Lake Tahoe, CA, Oct. 15, 2001. **\*invited**
5. Thin Gate Oxide Reliability  
J. S. Suehle and E. M. Vogel  
International Reliability Physics Symposium, Apr. 10, 2000. **\*invited**

*Industry/University Colloquia (\*14 invited)*

1. Electrical and Physical Properties of High-k Gate Dielectrics on III-V Semiconductors  
E. M. Vogel  
IBM TJ Watson Research Center, Physical Sciences Seminar, Oct. 24, 2008. **\*invited**
2. Biosensing Using Semiconductor Technologies  
W. Hu, E. M. Vogel, J. Gao, and B. Sumer  
IEEE-Dallas Chapter of Engineering in Medicine and Biology Society (EMBS), Feb. 19, 2007. **\*invited**
3. Initiatives in Nanometrology  
E. M. Vogel and W. Hu  
Texas Instruments, Dallas, TX, Jan. 8, 2007. **\*invited**
4. Method for Measuring the Barrier Height at the High-k/Metal Electrode Interface, and Combinatorial Determination of Optimal Metal Gate Electrodes  
M. Green and E. M. Vogel  
SEMATECH Advanced Gate Stack Engineering Working Group Biannual Meeting, Austin, TX, Feb. 14, 2005. **\*invited**

5. Depth Profiles of Electrically Active Defects in High-k Gate Stacks Using Charge Pumping  
E. M. Vogel and D. Heh  
SEMATECH Advanced Gate Stack Engineering Working Group Biannual Meeting, Austin, TX, Feb. 15, 2005. **\*invited**
6. Characterization Needs for Emerging Research Materials and Devices  
Eric M. Vogel  
ITRS Emerging Research Materials Workshop, San Francisco, CA, July 11, 2004. **\*invited**
7. Computational Needs for Emerging Materials: An Experimental Metrologist's Viewpoint  
Curt A. Richter and Eric Vogel  
Materials Modeling for Emerging Research Materials Workshop, Austin, TX, June 7, 2004.  
**\*invited**
8. Challenges of Electrical Measurements of Advanced Gate Dielectrics in MOS Devices  
E. M. Vogel  
Applied Materials, Feb. 9, 2004. **\*invited**
9. NIST Response to ITRS and Beyond  
E. M. Vogel and D. Blackburn  
SRC Metrology Needs for Emerging Technologies Workshop, Raleigh, NC, May 3, 2002.  
**\*invited**
10. Reliability of Ultra-thin Silicon Dioxide for Future MOS Devices  
E. M. Vogel  
Penn State University, Dept. of Engineering Science, Oct. 4, 2000. **\*invited**
11. Capacitance and Conductance Characterization of MOS Capacitors with Tunneling Gate Dielectrics  
Eric M. Vogel  
SEMATECH Gate Stack Engineering Working Group Meeting, Raleigh, NC, November 11, 1999. **\*invited**
12. Electrical Characterization and Reliability of MOS Devices with Tunneling Gate Dielectrics  
E. M. Vogel  
IBM, Yorktown Heights, NY, October 14, 1999. **\*invited**
13. Alternate Dielectric Technology and Metrology  
E. M. Vogel  
University of Delaware, Dept. of Electrical and Computer Engineering, July 13, 1999.  
**\*invited**
14. Reliability of Ultrathin Oxides for MOS Devices  
E. M. Vogel  
North Carolina State University, Dept. of Electrical and Computer Engineering, Apr. 22, 1999. **\*invited**

Conferences (\*23 invited)

1. In-situ XPS investigation of the “clean-up” effect through half-cycle ALD reactions on III-V substrates  
M. Milojevic, B. Brennan, F. S. Aguirre-Tostado, C. Hinkle, H. C. Kim, B. Lee, G. Hughes, E. M. Vogel, J. Kim, and R. M. Wallace  
IEEE Semiconductor Interface Specialists Conference, 2008.
2. Performance Enhancement of n-Channel Inversion Type In<sub>x</sub>Ga<sub>1-x</sub>As MOSFET by Effective Surface Passivation Using Ex-Situ Deposited Thin Amorphous Si Layer  
A. M. Sonnet, C. L. Hinkle, M. N. Jivani, J. Kim, R. A. Chapman, R. M. Wallace and E. M. Vogel  
IEEE Semiconductor Interface Specialists Conference, 2008.
3. Surface states, interface traps, and Fermi level pinning correlation to the interface oxidation states of Ga  
C. L. Hinkle, A. M. Sonnet, E. M. Vogel, M. Milojevic, F. S. Aguirre-Tostado, J. Kim, R. M. Wallace, B. Brennan, and G. J. Hughes  
IEEE Semiconductor Interface Specialists Conference, 2008.
4. Electrical and Physical Properties of High-k Gate Dielectrics on III-V Semiconductors  
E. M. Vogel, C. L. Hinkle, A. Sonnet, F. S. Aguirre-Tostado, M. Milojevic, K. J. Choi, H. C. Kim, J. G. Wang, H. C. Floresca, J. Kim, M. J. Kim, and R.M. Wallace  
American Vacuum Society Meeting, 2008. **\*invited**
5. Electrical and Physical Properties of GaAs MOS Devices with Al<sub>2</sub>O<sub>3</sub>/a-Si Gate Dielectric Stacks  
Eric M. Vogel, A. Sonnet, C. L. Hinkle, F. S. Aguirre-Tostado, M. Milojevic, J. Kim, and R.M. Wallace.  
5th International Symposium on Advanced Gate Stack Technology, 2008. **\*invited**
6. Comparison of n-type and p-type GaAs oxide growth and its effects on frequency dispersion characteristics  
C. L. Hinkle, A. M. Sonnet, M. Milojevic, F. S. Aguirre-Tostado, H. C. Kim, J. Kim, R. M. Wallace, and E. M. Vogel  
Workshop on Dielectrics in Microelectronics, 2008.
7. Study of surface preparation for high-k dielectrics on GaAs  
F. S. Aguirre-Tostado, M. Milojevic, S. McDonnell, R. Contreras-Guerrero, C. L.Hinkle, K. J. Choi, J. Kim, E. M. Vogel, A. Herrera-Gomez, R. M. Wallace, T. Yang, Y. Xuan and P.D. Ye  
IEEE Semiconductor Interface Specialists Conference, 2007.
8. GaAs MOS Frequency Dispersion Reduction by Surface Oxide Removal and Passivation  
C. L. Hinkle, A. M. Sonnet, E. M. Vogel, S. McDonnell, M. Milojevic, B. Lee, F. S. Aguirre-Tostado, K. J. Choi, J. Kim and R. M. Wallace

IEEE Semiconductor Interface Specialists Conference, 2007.

9. Characterization of Electrically Active Interfacial Defects in High- $\kappa$  Gate Dielectrics  
E. M. Vogel, A. M. Sonnet, and C. L. Hinkle  
Electrochemical Society Meeting, 2007. **\*invited**
10. GaAs Surface Modification by Arsenic Oxide Removal and Bond Conversion  
C. L. Hinkle, M. Milojevic, S. McDonnell, F. S. Aguirre-Tostado, A. M. Sonnet, R. M. Wallace, and E. M. Vogel  
4th International Symposium on Advanced Gate Stack Technology, Dallas, TX, Sept. 27, 2007.
11. Metrology for Emerging Devices and Materials  
E. M. Vogel  
American Materials Failure Analysis (AMFA) Workshop, Phoenix, AZ, April 20, 2007.  
**\*invited**
12. Metrology for Beyond CMOS: Emerging Devices and Materials  
E. M. Vogel  
53<sup>rd</sup> American Vacuum Society International Symposium, Nano-Manufacturing Topical Conference, San Francisco, CA, Nov. 12-16, 2006. **\*invited**
13. Technology and Metrology for Beyond CMOS  
E. M. Vogel  
SEMATECH-SRC Topical Research Conference on Reliability, Austin, TX, Oct. 23, 2006.  
**\*invited**
14. Precise Manipulation and Alignment of Single Nanowires for Device Fabrication  
Q. Li, S.-M. Koo, C. A. Richter, M. D. Edelstein, J. J. Kopanski, J. S. Suehle, and E. M. Vogel  
2006 IEEE Silicon Nanoelectronics Workshop, Honolulu, HI, June 11-12, 2006.
15. Schottky-contact silicon nanowire field effect transistor test structures  
S.-M. Koo, C. A. Richter, Q. Li, M. D. Edelstein, and E. M. Vogel  
2006 IEEE Silicon Nanoelectronics Workshop, Honolulu, HI, June 11-12, 2006.
16. Work function characterization of TaSiN and TaCN electrodes using CV, IV, IPE and SKPM  
H. D. Xiong, N. V. Nguyen, J. J. Kopanski, J. S. Suehle, and E. M. Vogel  
Electrochemical Society Meeting, 2006.
17. Detection of Electron Trap Generation Due to Constant Voltage Stress on High- $\kappa$  Gate Stacks  
C. D. Young, S. Nadkarni, D. Heh, H. R. Harris, R. Choi, J. J. Peterson, J. H. Sim, S. A. Krishnan, J. Barnett, E. Vogel, B.H. Lee, P. Zeitzoff, G. A. Brown, and G. Bersuker  
IEEE International Reliability Physics Symposium, 2006.

18. Metrology for new microelectronic materials  
E. M. Vogel  
American Physical Society Spring Meeting, Baltimore, MD, March 14, 2006. **\*invited**
19. Electrical Characterization of Defects in High-k Gate Dielectrics  
E. M. Vogel  
International Semiconductor Device Research Symposium, Bethesda, MD, Dec. 7, 2005.  
**\*invited**
20. Detection of trap generation in high-kappa gate stacks  
C. D. Young, S. Nadkarni, D. Heh, H. R. Harris, R. Choi, J. J. Peterson, J. H. Sim, S. A. Krishnan, J. Barnett, E. Vogel, B.H. Lee, P. Zeitzoff, G. A. Brown, and G. Bersuker  
IEEE Integrated Reliability Workshop, 2005
21. Physical Mechanisms of Ultra-thin Silicon Dioxide Degradation and Breakdown  
E. M. Vogel  
Electrochemical Society Meeting, 2005. **\*invited**
22. Comparison of scanning capacitance microscopy and scanning Kelvin probe microscopy in determining two-dimensional doping profiles of Si homostructures  
S.-E. Park, N. V. Nguyen, J. J. Kopanski, J. S. Suehle, and E. M. Vogel,  
Ultra Shallow Junction Conference, Daytona Beach, FL, 2005.
23. Characterization of electrically active defects in high-k gate dielectrics using charge pumping  
E. M. Vogel and D. Heh  
NATO Advanced Research Workshop on Defects in Advanced High-k Dielectric Nanoelectronic Semiconductor Devices, 2005. **\*invited**
24. Electrical Characterization of MOS structures and Wide Bandgap Semiconductors by Scanning Kelvin Probe Microscopy  
S.-E. Park, St. Jeliaskov, J. J. Kopanski, J. Suehle, E. Vogel, A. Davydov, and H.-K. Shin  
MRS Spring Meeting, San Francisco, CA, 2005.
25. Metrology for Emerging Research Devices and Materials  
E. M. Vogel  
Characterization and Metrology for ULSI Technology Conference, 2005. **\*invited**
26. The Contribution of HfO<sub>2</sub> Bulk Oxide Traps to Dynamic NBTI in pMOSFETs  
B. Zhu, J. S. Suehle, E. Vogel, and J. B. Bernstein  
IEEE International Reliability Physics Symposium, 2005.
27. A Perspective on the Future of Electronics  
E. M. Vogel  
Nano 2004, Baltimore, MD, Nov. 12, 2004. **\*invited**

28. Reverse Short Channel Effects in High-k Gated nMOSFETs  
J.-P. Han, S. M. Koo, E. M. Vogel, E. P. Gusev, C. D'Emic, C. A. Richter, and J. S. Suehle  
13<sup>th</sup> Workshop on Dielectrics in Microelectronics, Kinsale, Ireland, June 28, 2004.
29. Characterization of Structural Quality of Bonded Silicon-on-Insulator Wafers by Spectroscopic Ellipsometry and Raman Spectroscopy  
N. V. Nguyen, J. E. Maslar, J.-Y. Kim, J.-P. Han, J.-W. Park, D. Chandler-Horowitz, and E. M. Vogel  
Materials Research Society Meeting, 2004.
30. New Insights into Threshold Voltage Shifts for Ultrathin Gate Oxides  
D. Heh, E. M. Vogel, and J. B. Bernstein  
IEEE Integrated Reliability Workshop, 2004.
31. Influence of Buffer Layer Thickness on the Ferroelectric Memory window of SrBi<sub>2</sub>Ta<sub>2</sub>O<sub>9</sub>/SiN/Si Structure  
Jin-Ping Han, S.M. Koo, C. A. Richter and Eric Vogel,  
16<sup>th</sup> international Symposium on Integrated Ferroelectrics (ISIF'04), Gyeongju, Korea, April 5-8, 2004.
32. Challenges of Electrical Measurements of Advanced Gate Dielectrics in Metal-Oxide-Semiconductor Devices  
E. M. Vogel, and G. A. Brown  
International Conference on Characterization and Metrology for ULSI Technology, 2003.  
**\*invited**
33. Thickness evaluation for 2 nm SiO<sub>2</sub> films, a comparison of ellipsometric, capacitance-voltage and HRTEM measurements  
J. Ehrstein, C. Richter, D. Chandler-Horowitz, E. Vogel, D. Ricks, C. Young, S. Spencer, S. Shah, D. Maher, B. Foran, A. Diebold, and P. Y. Hung  
International Conference on Characterization and Metrology for ULSI Technology, 2003.
34. Characterization of ultrathin amorphous silicon and correlation with crystalline evolution after thermal annealing  
J. Park, C. A. Richter, J. Y. Kim, N. V. Nguyen, J. E. Bonevich, and E. M. Vogel  
MRS Spring Meeting, 2003.
35. Energy Distribution of Interface Traps in High-k Gated MOSFETs  
J.-P. Han, E. M. Vogel, E. P. Gusev, C. D'Emic, C. A. Richter, D. Heh, and J. Suehle  
Symposium on VLSI Technology, 2003.
36. Defect Generation in Ultra-thin Oxide Over Large Fluence Ranges  
D. Heh, J. B. Bernstein, and E. M. Vogel,  
IEEE Integrated Reliability Workshop, 2002.
37. Issues with Electrical and Reliability Characterization of Advanced Gate Dielectrics,

E. M. Vogel

5<sup>th</sup> Topical Research Conference on Reliability, Austin, TX, Oct. 28, 2002. **\*invited**

38. Relevance of injected hot holes on the breakdown of ultra-thin silicon-dioxide metal-semiconductor devices  
D. Heh, E. M. Vogel, and J. Bernstein  
American Physical Society Spring Meeting, Indianapolis, IN, March 21, 2002.
39. Issues with Electrical and Reliability Characterization of Advanced Gate Dielectrics  
E. M. Vogel  
Proceedings of the 12<sup>th</sup> Workshop on Dielectrics in Microelectronics, Grenoble, France, Nov. 20, 2002. **\*invited**
40. Degradation and breakdown of ultra-thin silicon dioxide by electron and hole injection  
E. M. Vogel,  
IEEE Microelectronics Reliability and Qualification Workshop, Glendale, CA, Dec. 11, 2001.  
**\*invited**
41. Interaction of Electrons with Defects Created by Hot Holes in Ultra-thin Silicon Dioxide  
E. M. Vogel, D. Heh, B. Wang, C. E. Weintraub, J. S. Suehle, M. D. Edelstein, and J. B. Bernstein, 32<sup>nd</sup> IEEE Semiconductor Interface Specialists Conference, Washington D.C., Nov. 29, 2001.
42. Latent Reliability Degradation of Ultra-Thin Oxides After Heavy Ion and  $\gamma$  -ray Irradiation  
B. Wang, J. S. Suehle, J. F. Conley, Jr., E. M. Vogel, C. E. Weintraub, A. H. Johnston, and J. B. Bernstein  
IEEE Integrated Reliability Workshop, 2001.
43. Differences between Quantum-Mechanical Capacitance-Voltage Simulators  
C. A. Richter, E. M. Vogel, A. M. Hodge, and A.R. Hefner,  
International Conference on Simulation of Semiconductor Processes and Devices, Athens, Greece, Sept. 5-7, 2001.
44. Issues with the Electrical Characterization and Reliability of MOS Devices With Advanced Gate Dielectrics  
E. M. Vogel  
Materials Research Society Workshop on Dielectric Science & New Functionality in Device Physics for Crystalline Oxides on Semiconductors (COS), Chattanooga, TN, September 11, 2001. **\*invited**
45. Reliability of Ultra-thin Silicon Dioxide Under Substrate Hot-electron, Substrate Hot-hole, and Tunneling Stress  
E. M. Vogel, M. D. Edelstein, and J. S. Suehle  
12<sup>th</sup> Insulating Films on Semiconductors Conference, Udine, Italy, June 20-23, 2001.  
**\*invited**

46. Challenges of High- $\kappa$  Gate Dielectrics for Future MOS Devices  
J. S. Suehle, E. M. Vogel, M. D. Edelstein, C. A. Richter, N. V. Nguyen, I. Levin, and D. L. Kaiser, H. Wu, and J. Bernstein  
6<sup>th</sup> International Symposium on Plasma and Process-Induced Damage, Monterey, CA, May 13-15, 2001.
47. Degradation and Breakdown of Ultra-thin Silicon Dioxide Induced by Substrate Hot Hole Injection  
E. M. Vogel and J. S. Suehle  
31<sup>st</sup> IEEE Semiconductor Interface Specialists Conference, San Diego, CA, Dec. 7-9, 2000.
48. The Effect of Stress Interruption and Pulsed Bias Stress on Ultra-thin Gate Dielectric Reliability  
B. Wang, J. S. Suehle, E. M. Vogel, and J. B. Bernstein  
IEEE International Integrated Reliability Workshop, 2000.
49. Issues in High- $\kappa$  Gate Dielectrics for Future MOS Devices  
E. M. Vogel, M. D. Edelstein, C. A. Richter, N. V. Nguyen, I. Levin, D. L. Kaiser, H. Wu, and J. Bernstein  
IEEE Microelectronics Reliability and Qualification Workshop, Glendale, CA, Oct. 31, 2000.  
**\*invited**
50. The Effects of Ionizing Radiation on Wear-out and Reliability of Thin Gate Oxides  
J. S. Suehle, T. Myers, M. Edelstein, E. M. Vogel, and J. F. Conley, Jr.,  
IEEE Microelectronics Reliability and Qualification Workshop, Glendale, CA, Oct. 31, 2000.
51. High- $\kappa$  Gate Dielectric Reliability – Issues in Characterization, Physical Modeling, and Assessment  
E. M. Vogel  
Materials Research Society High- $\kappa$  Gate Dielectric Workshop, New Orleans, LA, June 1-2, 2000. **\*invited**
52. Temperature Dependence of Soft Breakdown and Wear-Out in Sub 3 nm SiO<sub>2</sub> Films  
J. S. Suehle, E. M. Vogel, B. Wang, and J. B. Bernstein  
IEEE International Reliability Physics Symposium, 2000.
53. Panel presentation on “Is technology scaling limited by oxide reliability?”  
E. M. Vogel  
International Reliability Physics Symposium, Apr. 13, 2000. **\*invited**
54. Extraction of the Gate Oxide Thickness of N- and P-Channel MOSFETs Below 20 Å from the Substrate Current Resulting from Valence-Band Electron Tunneling  
A. Shanware, J. P. Shiely, H. Z. Massoud, E. Vogel, K. Henson, A. Srivastava, C. Osburn, J. R. Hauser, and J. J. Wortman  
International Electron Device Meeting, 1999.

55. Degradation of Ultra-thin SiO<sub>2</sub> Under Combined Substrate Hot Electron and Tunneling Stress  
E. M. Vogel, J. S. Suehle, M. D. Edelstein, B. Wang, Y. Chen, and J. B. Bernstein  
30<sup>th</sup> IEEE Semiconductor Interface Specialists Conference, Charleston, SC, December 2-4, 1999.
56. Sheet and Line Resistance of Patterned SOI Surface Film CD Reference Materials as a Function of Substrate Bias  
R. A. Allen, E. M. Vogel, L. W. Linholm, and M. W. Cresswell  
IEEE International Conference on Microelectronic Test Structures, 1999.
57. *In Situ* Diffuse Reflectance Spectroscopy for Measurement and Control of III-V Molecular Beam Epitaxy  
J. E. Guyer, W. F. Tseng, W. R. Thurber, E. M. Vogel, D. A. Gajewski, and J. G. Pellegrino  
Materials Research Society Fall Meeting, Boston, MA, Nov. 29 - Dec. 3, 1999.
58. Properties of N- and P-Channel MOSFETs with Ultrathin RTCVD Oxynitride Gate Dielectrics  
E. M. Vogel, and J. J. Wortman  
Electrochemical Society Spring Meeting, Seattle, Washington, May 2-7, 1999. **\*invited**
59. MOSFET Substrate Currents due to Valence-Band Tunneling in 15-35 Å  
A. Shanware, H. Z. Massoud, E. Vogel, K. Henson, J. R. Hauser, and J. J. Wortman  
29<sup>th</sup> IEEE Semiconductor Interface Specialists Conference, San Diego, CA, December 3-5, 1998.
60. Properties of n-Channel and p-Channel MOSFETs with Ultrathin Gate Dielectrics  
E. M. Vogel, C. E. Weintraub, and J. J. Wortman  
SRC TECHCON '98, Las Vegas, NV, September 9-11, 1998.
61. Evaluation of 2.0 nm Grown and Deposited Dielectrics in 0.1 μm PMOSFETs  
A. Srivastava, H. H. Heinisch, E. Vogel, C. Parker, C. M. Osburn, N. A. Masnari, J. J. Wortman, and J. R. Hauser  
Materials Research Society Meeting, 1998.
62. E. M. Vogel, J. J. Wortman, and J. R. Hauser,  
The Use of RTCVD Oxynitrides in Ultra-thin Gate Dielectric Stacks  
28<sup>th</sup> IEEE Semiconductor Interface Specialists Conference, Charleston, SC, December 4-6, 1997.
63. Silicon oxynitride films formed by rapid thermal chemical vapor deposition for VLSI applications  
E. M. Vogel, J. J. Wortman, P. K. McLarty, V. H. C. Watt, and B. Kirkpatrick  
ECS Symposium on Silicon Nitride and Silicon Dioxide Thin Insulating Films, 1997.  
**\*invited**
64. Stacked RTCVD Oxide and Oxynitride Films for Ultrathin Gate Dielectrics

E. M. Vogel, W. K. Henson, P. K. McLarty, J. J. Wortman, and J. R. Hauser,  
27<sup>th</sup> IEEE Semiconductor Interface Specialists Conference, San Diego, CA, December 5-7,  
1996.

65. A self-consistent physical explanation for the mobility behavior of n-channel and p-channel MOSFETs with oxynitride gate dielectrics formed by low pressure rapid thermal chemical vapor deposition  
E. M. Vogel, W. L. Hill, V. Misra, P. K. McLarty, J. J. Wortman, J. R. Hauser, P. Morfouli, G. Ghibaudo, and T. Ouisse  
26<sup>th</sup> IEEE Semiconductor Interface Specialists Conference, Charleston, SC, December 7-9, 1995.
66. Electrical and Reliability Properties of Thin Silicon Oxynitride Dielectrics Formed by Low Pressure Rapid Thermal Chemical Vapor Deposition  
P. Morfouli, G. Ghibaudo, E. M. Vogel, W. L. Hill, V. M. Misra, P. K. McLarty, and J. J. Wortman  
Proceedings of the 7<sup>th</sup> ESPRIT Workshop on Dielectrics in Microelectronics, Crete, Greece, November, 1995.
67. Noise Analysis of MOSFET's with Ultra Thin Silicon Oxynitride Films Prepared by Low Pressure Rapid Thermal Chemical Vapor Deposition (LPRTCVD)  
P. Morfouli, G. Ghibaudo, T. Ouisse, E. M. Vogel, W. L. Hill, V. Misra, P. McLarty, J. J. Wortman  
Proceedings of the 25<sup>th</sup> European Solid State Device Research Conference, Hague, Netherlands, September 25-27, 1995.

**External funding for original investigations  
(Vogel individual portion of external funding currently >\$700k/yr):**

**The University of Texas at Dallas**

**Active**

1. MOS Transistor Process Integration and device characterization of high-k / metal gate stacks on InGaAs  
R. M. Wallace (Lead), E. M. Vogel, J. Kim  
SEMATECH  
6/2008-11/2008, Total: \$100k/1.0 yr, Vogel: \$50k/yr.
2. UTD-Korea collaborative research on Future Semiconductor commercializatiON (FUSION)  
M. Kim (Lead), J. Kim (Lead), B. Gnade, R. Wallace, E. Vogel, K. Cho  
Texas Emerging Technology Fund (COSAR/MOCIE)  
09/2007-08/2011, Total: \$5M/4 yrs, Vogel: ~\$200k/yr.
3. Lithographically defined nanoscale silicon sensors for cancer diagnostics  
W. Hu (Lead), E. M. Vogel, J. Gao, and B. Sumer  
Texas Instruments Medical Electronics,  
4/2008-4/2009, Total: \$200k/1 yr, Vogel: \$50k/yr.
4. Nanoelectronic Devices and Materials for a Neuro-inspired Architecture  
E. M. Vogel (Lead)  
Southwest Academy for Nanoelectronics (Director: S. Banerjee, UT-Austin)  
Semiconductor Research Corporation (SRC) Nanoelectronics Research Initiative  
4/2008-4/2011, Total: \$250k/3 yrs, Vogel: \$83k/yr.
5. Realization and characterization of graphene-based materials and device  
E. M. Vogel (Lead), M. J. Kim, J. Kim, R. M. Wallace, B. E. Gnade, K. J. Cho, Y. Chabal  
Southwest Academy for Nanoelectronics (Director: S. Banerjee, UT-Austin)  
Semiconductor Research Corporation (SRC) Nanoelectronics Research Initiative and Texas Emerging Technology Fund  
4/2008-4/2011, Total: \$950k/3 yrs, Vogel: \$50k/yr.
6. PMOS Metal Gate Electrodes on High-k Dielectrics  
H. Alshareef (Lead), E. M. Vogel, R. M. Wallace, J. Kim, B. Gnade, C. Hinkle  
Texas Instruments  
2/2008-2/2009, Total: \$140k/1 yr, Vogel: \$85k/yr.
7. Capacitance-Voltage Methods for Alternative Channel Devices  
E. M. Vogel (Lead)  
SEMATECH  
12/2007-12/2008, Vogel: \$55k/1 yr.
8. UTD-Korea collaborative research on Future Semiconductor commercializatiON (FUSION)

M. Kim (Lead), J. Kim (Lead), B. Gnade, R. Wallace, E. Vogel, K. Cho  
Korea Electronic Technology Institute (COSAR/MOCIE)  
09/2007-08/2011, Total: \$6M/4 yrs, Vogel: \$125k/yr.

9. Metrology for Extreme CMOS Devices  
E. M. Vogel (Lead)  
National Institute of Standards and Technology  
09/2006-08/2009, Total: \$345k/3 yrs, Vogel: \$115k/yr

**Declined**

1. EMT/MISC: Nanoscale Materials and Devices for an Ultimately Scalable Silicon Neuron  
E. M. Vogel (Lead), J. Kim, W. Hu  
NSF  
09/2008-09/2011, Total: \$500k/3 yrs
2. Nanoscale Materials and Devices for an Ultimately Scalable Silicon Neuron  
E. M. Vogel (Lead), J. Kim, W. Hu  
NSF  
09/2008-09/2011, Total: \$300k/3 yrs
3. Active Interconnects for a Scalable Neuromorphic Architecture: Foundation for an Intelligent Machine  
E. M. Vogel (Lead), D. Allstot, J. Kim, W. Hu, P. Abshire (UMd), J. George (LANL), G. Kenyon (LANL), J. Galbraith (LANL), D. Halladay (ATDF), ...  
DARPA (BAA 08-28)  
09/2008-06/2015, Total: \$120M/7 yrs, Phase 0: \$1.5 M
4. MRI: Development of an Integrated Facility for in-situ characterization of interfaces and nanostructured materials  
Y. Chabal (Lead), K. Cho, J. Kim, E. M. Vogel, R. M. Wallace  
NSF  
07/2008-07/2010, Total: \$260k/2 yrs
5. Nano-scale Amorphous Silicon Devices for a CMOS-compatible Neuro-inspired Architecture  
E. M. Vogel (Lead)  
Texas Advanced Research Program  
06/2008-06/2010, Total: \$150k/2 yrs
6. Variability and Reliability of Pentacene-based Organic Field-Effect-Transistors and Circuits”  
E. M. Vogel (Lead), R. M. Wallace, K. J. Cho  
NSF  
09/2007 – 09/2010, Total: \$325k/3 yrs
7. Radiation Hardened High- $\kappa$  Gate Dielectrics

E. M. Vogel (Lead), J. Y. Kim, R. M. Wallace  
Air Force Research Laboratory - BAA-VS-06-05  
06/2007 – 06/2009, Total: \$130k/2 yrs

8. Active Interconnects for a Neuro-inspired Architecture on a Silicon Platform  
E. M. Vogel (Lead)  
Semiconductor Research Corporation – Cross-disciplinary Semiconductor Research  
09/2007 - 09/2008, Total: \$40k/1 yr
9. GOALI: Collaborative Research on High-k Dielectrics on III-V Compound Semiconductors  
R. M. Wallace (Lead), K. J. Cho, J. Kim, P. Pinsukanjana, E. M. Vogel  
NSF  
07/2008 – 07/2011, Total: \$888k/3 yrs
10. White Paper: Nano-scale Devices with Emerging Materials for a CMOS-compatible Neuro-inspired SOC Architecture  
E. M. Vogel (Lead), J. Kim, W. Hu  
Semiconductor Research Corporation – GRC Call for White Papers  
09/2007 - 09/2010, Total: \$450/3 yrs
11. White Paper: Reliability of GaN High Voltage Devices  
E. M. Vogel (Lead), M. J. Kim, P. Saunier, U. Chowdhury, J. Suehle  
Air Force Office for Scientific Research (BAA 07-036)  
01/2008 – 01/2011, Total: \$1M/3 yrs
12. White Paper: Devices for a Neuro-inspired Architecture on a Silicon Platform  
E. M. Vogel (Lead)  
Air Force Research Laboratory – Rome (BAA-04-03-IFKA)  
09/2007 – 09/2009, Total: \$300k/2 yrs
13. White Paper: Nano-scale Non-crystalline Silicon Devices for a CMOS-compatible Neuro-inspired SOC Architecture  
E. M. Vogel (Lead)  
Air Force Research Laboratory – Wright (BAA-07-01 PKD)  
09/2007 – 09/2009, Total: \$300k/2 yrs
14. White Paper: Amorphous Silicon Devices for a CMOS-compatible Neuro-inspired Architecture  
E. M. Vogel (Lead)  
Army Research Office (BAA W911NF-07-R-0001)  
09/2007 – 09/2010, Total: \$450k/3 yrs
15. White Paper: Impact of Radiation on High- $\kappa$  Gate Dielectrics  
E. M. Vogel (Lead), R. M. Wallace, J. Kim  
Naval Surface Warfare Center, Crane Division (BAA N00164-06-R-6533)  
09/2007 – 09/2009, Total: \$275k/2 yrs

16. GOALI: Collaborative Research on High-k Dielectrics on III-V Compound Semiconductors  
R.M.Wallace (Lead), J. Kim, E. Vogel, P. Pinsukanjana, K. Cho  
NSF  
08/2007-07/2010, Total: \$730k/3 yrs
17. Nanoscholar internship program / Nanoelectronics workforce development initiative  
J. Kim (Lead), M. Kim, E. M. Vogel, R. M. Wallace  
Sematech/ACC  
01/2007 – 01/2008, Total: \$81k/1 yr
18. MOSFETs with High-k Gate Dielectrics for Radiation Dosimeters  
E. Vogel (PI), J. Kim, H. Hamidian  
UTD-UTSW  
04/2007-03/2008, Total: \$100k/1 yr

**National Institute of Standards and Technology (5/98 – 5/06)**

1. Methodology for Measuring Work Functions and Band Offsets of the High- $\kappa$ /Metal Gate Electrode Stack, and Combinatorial Determination of Optimal Metal Gate Electrodes  
E. M. Vogel, M. Green, J. Suehle  
SEMATECH  
2005, \$250k/1 year
2. Development of Backside FTIR for the High-k/Metal Gate Stack  
E. M. Vogel, C. Hacker, A. Chaka, E. Jarvis  
SEMATECH  
2005, \$50k/1 year
3. Development and Validation of Molecular Electronics Test Structures  
R. Van Zee, C. A. Richter, J. D. Batteas, M. J. Tarlov, E. M. Vogel  
DARPA MoleApps  
2004, \$1M/5 years
4. The Use of Charge Pumping for Measuring Electrically Active Defects in High-k Gate Dielectrics  
E. M. Vogel  
SEMATECH  
2004, \$50k/1 year
5. C-V Measurements of Oxide Thickness  
E. M. Vogel  
SEMATECH  
2003, \$50k/1 year
6. Electrical Characterization of Advanced Gate Dielectrics

E. M. Vogel  
SEMATECH  
2002, \$50k/1 year

**Teaching:**

**Doctoral advisement/direction:**

1. Dawei Heh, Ph.D. May 2005, Univ. of Maryland, Dept. of Electrical Engineering (Performed entire PhD research under my advisement at NIST).
2. Poornika Fernandes, Sept. 2006 – present (Passed QE Dec. 2007, Proposal planned Spr 09)
3. Arif Sonnet, Sept. 2006 – present (Passed QE Dec. 2007, Proposal planned Spring 2009)
4. Kurtis Cantley, Sept. 2007 – present (Passed QE March 2008, Proposal planned Spring 2009)
5. Archana Venugopal, Oct. 2007 – present (QE planned March 2009)
6. Rohit Galatage, Jan. 2008 – present (QE planned Dec. 2008)

**Master's advisement/direction:**

1. Naqi Jivani, Sept. 2008 – present (M.S. planned Dec. 2009)
2. Shreyasee Dey, Jan. 2007 – present (M.S. planned Dec. 2008)
3. Ram Pratiwadi (M.S. Aug. 2008)

**Undergraduate advisement/direction:**

1. Naqi Jivani, Jan. 2007 – Aug. 2008
2. David Rico, May 2008 – present

**Post-doctoral advisement/direction:**

1. Chris Hinkle, Nov. 2006 – present

**Technical staff supervision:**

1. Jim Burris (process technician), June 2008 - present

**Classroom teaching:**

2008, Fall

Special Topics in Microelectronics: Semiconductor Device Characterization, EE 7V82, 10 students (3 credits)

Course as a whole: N/A, Course content: N/A, Instructor: N/A at time of submission

2008, Spring

Electronic Circuits Laboratory, EE 3111, 57 students (1 credit)

Course as a whole: 3.73/5, Course content: 3.63/5, Instructor: 3.66/5

2007, Fall

Fundamentals of Semiconductor Devices, EE/MSEN-6320-501, 23 students (3 credits)

Course as a whole: 3.57/5, Course content: 3.65/5, Instructor: 3.22/5

2006, Fall

Fundamentals of Semiconductor Devices, EE/MSEN-6320-501, 10 students (3 Credits)

Course as a whole: 3.6/5, Course content: 4.0/5, Instructor: 3.4/5

Research and thesis

2008, Fall

Research in EE, EE-8V70-080, 4 students (6 credits)

2008, Fall

Thesis, EE-8V98-080, 1 student (6 credits)

2008, Summer

Research in EE, EE-8V70-080, 6 students (6 credits)

2008, Summer

Thesis, MSEN-8V98-080, 1 student (6 credits)

2008, Spring

Research in EE, EE-8V70-080, 1 student (9 Credits), 2 students (6 Credits), 1 student (3 credits)

2008, Spring

Research in MSEN, MSEN-8V70-080, 1 student (3 credits)

2008, Spring

Thesis, MSEN-8V98-080, 1 student (6 credits)

2007, Fall

Research in EE, EE-8V70-080, 4 students (3 credits)

2007, Summer

Research in EE, EE-8V70-080, 3 students (6 credits)

2007, Summer

Research in MSEN, MSEN-8V70-080, 2 students (6 credits)

2007, Spring

Research in EE, EE-8V70-080, 2 students (3 credits)

**Administration and curricula development:**

2008, Fall

Semiconductor Device Characterization, EE/MSEN 7V82

This new course will be offered this fall. The syllabus is attached.

2009, Spring

Introduction to Nanotechnology, NANO 3301

This new course will be offered next spring. The syllabus is attached.

**Service – reviewing, refereeing and administrative work with professional societies and organizations; departmental, college, university committees; community service:**

Conference Committees:

2008

- *Chair*, High-k Program Committee, 2008 IEEE International Reliability Physics Symposium

2007

- *Co-organizer*, FIAP Focus Session on Emerging Research Devices and Materials for the Microelectronics Industry, 2007 American Physical Society Spring Meeting
- Member, High-k Program Committee, 2007 IEEE International Reliability Physics Symposium

2006

- Member, Program Committee, 2006 Workshop on Dielectrics in Microelectronics
- *Ex-Officio Chair*, 2006 Semiconductor Interface Specialists Conference

2005

- *General Chair*, 2005 Semiconductor Interface Specialists Conference

2004

- *Technical Chair*, 2004 Semiconductor Interface Specialists Conference

2003

- Member, Dielectrics Program Committee, 2003 IEEE International Reliability Physics Symposium
- *Arrangements Chair*, 2003 Semiconductor Interface Specialists Conference

2002

- Member, Dielectrics Program Committee, 2002 IEEE International Reliability Physics Symposium
- Member, Technical Program Committee, 2002 Semiconductor Interface Specialists Conference
- Member, Technical Program Committee, 2002 IEEE Integrated Reliability Workshop

2001

- *Co-Chair*, Dielectrics Program Committee, 2001 IEEE International Reliability Physics Symposium
- Member, Technical Program Committee, 2001 Semiconductor Interface Specialists Conference
- Member, Technical Program Committee, 2001 IEEE Integrated Reliability Workshop

2000

- Member, Technical Program Committee, 2000 Semiconductor Interface Specialists Conference
- *Co-organizer*, 2000 MRS Workshop on High- $\kappa$  Gate Dielectrics

Industry Committees:

2004-2007

- International Technology Roadmap for Semiconductors, Emerging Research Materials Working Group

2000-2004

- International Technology Roadmap for Semiconductors, Front-End Processes Technical Working Group, 2000-2004

1998-2001

- SEMATECH Reliability Engineering Working Group
- SEMATECH Gate Stack Engineering Working Group

Journal Article and Other Reviews (since joining UTD):

2008

- *Evaluator for the Wittgenstein Award. The Wittgenstein Program was introduced in 1996 with the aim of funding outstanding scientists working in Austria and is managed by the Austrian Science Fund.*
- Reviewed five abstracts for the 2008 International Gate Stack Meeting
- Reviewed four abstracts for the 2008 International Electron Device Meeting.
- “Five-element circuit model using linear regression method to correct the admittance measurement of metal-oxide-semiconductor capacitor,” J. Vac. Sci. Technol. B, C.-C. Cheng et-al
- “Silicon nanowire dopant profiling and surface analysis via capacitance-voltage measurements,” Nature Nanotechnology, E. Garnett et al.
- “The Fermi Level Efficiency Method and its applications on high interface trap density oxide-semiconductor interfaces,” IEEE Elec. Dev. Lett., D. Lin et al.
- “Gate dielectrics and advanced channels for MOSFETs,” Superlattices and Microstructures, M. Wu et al.
- “Effect of interfacial SiO<sub>2</sub> layer on the ac conductance of HfO<sub>2</sub>/Si structures,” Appl. Phys. Lett., N. Miyata et al.
- “Complementary Symmetry Nanowire Logic Circuits: Experimental Demonstrations and In Silico Optimizations,” ACS Nano, J. Heath et al.

2007

- *Reviewer of Proposal to IEEE Transactions on Electron Devices for a Special Issues on Nanowire Transistors*
- “Electron Detrapping Characteristics in PBT-Stressed nMOSFETs with Ultrathin HfSiON Gate Dielectrics,” IEEE Elec. Dev. Lett., A. Nakajima et al.

- “Microstructure and Electrical Characteristics with Ferroelectric (Ba,Sr)TiO<sub>3</sub> Thin Films and HfO<sub>2</sub> Buffer Layer for the Non-Volatile Memory Application,” Surface Coatings and Technology, L.-C. Chang et al.
- “Interface Characterization and the Effect of Post-Deposition Anneal on Interfacial Properties of MOSFETs with HfO<sub>2</sub> Gate Dielectrics,” IEEE Elec. Dev. Lett., C.-H. Liu et al
- “Reliability characteristics of thick SiO<sub>2</sub> integrated with thin HfSiO<sub>x</sub> gate dielectric,” IEEE Elec. Dev. Lett., B-H Lee et al.
- “Extraction of the Threshold Voltage Shift by the Single Pulse Technique,” IEEE Elec. Dev. Lett., D. Heh et al.
- “Improvement in thermal stability of stacked structures of aluminum nitride and lanthanum oxide thin films on Si substrate,” Appl. Phys. Lett., D. Eom et al.
- “Investigation of the electronic structure at interfaces of crystalline and amorphous Gd<sub>2</sub>O<sub>3</sub> thin layers with silicon substrates of different orientations,” Appl. Phys. Lett., Mikhail Badylevich, et al.
- “A Unification of Interface-Trap Generation for Hot-carrier-injection in Low and High Voltage NMOSFET with Hole-trapping”, IEEE Elec. Dev. Lett., M. Zhi, et al.
- “On the effect of substrate bias on I-V and C-V characteristics of rf sputtered high dielectric hafnium oxide thin film,” J. Appl. Phys., R. K. Nahar et al.
- “Pulsed Id-Vg Methodology and Its Application to Electron Trapping Characterization and Defect Density Profiling,” IEEE Trans. Elec. Dev., C. Y. Young, et al.
- “Fundamental reliability of 1.5-nm-thick silicon oxide gate films grown at 150C by modified reactive ion beam deposition,” J. Appl. Phys., H. Ramada
- “Externally assembled gate-all-around carbon nanotube field-effect transistor,” IEEE Electron Device Letters, Z. Chen, et al.
- “Direct Observation of Electrically Active Interfacial Layer Defects Which May Cause Threshold Voltage Instabilities in HfO<sub>2</sub> Based MOSFETs,” Applied Physics Letters, J. Ryan, et al.
- "Si/a-Si Core/Shell Nanowires as Nonvolatile Crossbar Switches", NanoLetters, Yajie Dong, et al.
- "CMOS Compatible Nanoscale Non-Volatile Resistance Switching Memory", NanoLetters, Sung Hyun Jo, et al.

#### 2006

- “Impact of High K Gate Dielectrics on the Device and Circuit Performance of Nanoscale FinFETs,” IEEE Elec. Dev. Lett., V. Ramgopal Rao et al
- “Electron Detrapping Characteristics in PBT-Stressed nMOSFETs with Ultrathin HfSiON Gate Dielectrics,” IEEE Elec. Dev. Lett., A. Nakajima et al.
- “High-k Al<sub>2</sub>O<sub>3</sub>-HfTiO Nanolaminates with less than 0.8 nm equivalent oxide thickness,” IEEE Elec. Dev. Lett ,V. Mikhelashvili et al.

#### University Committees:

- *Chair*, MSEN Academic Search #7090, 2008-present
- *Chair*, Solid-state and Microsystems Faculty Concentration in Electrical Engineering, 2008-present
- *Co-Chair*, Nano Committee of EJS Industry Advisory Board, 2007-present

- Member, EE undergraduate curriculum committee, 2006-present

Special service contributions to Program, School, or University:

- July 24, 2008: Lecture for the Jonsson School Summer Program: “The Future of Semiconductors: From atoms to devices <or> Why math, physics, and chemistry are important for electrical engineers”
- July 8, 2008, Gave NSERL tour for the RHET 1101 summer program
- Feb. 2, 2008: EJS Graduate Student Recruiting Summit. Gave tours and met with potential students.
- Oct. 27, 2007: EJS Graduate Student Recruiting Summit. Gave tours and met with potential students.
- Oct.-Nov. 2007: Five (5) NSERL tours for incoming ECS freshmen
- Aug. 28, 2007: Gave NSERL tour to Louisiana Tech Delegates
- July, 2007: Lecture for the Jonsson School Summer Program: “The Future of Semiconductors: From atoms to devices <or> Why math, physics, and chemistry are important for electrical engineers”
- June 5, 2007: Gave NSERL tours for grand opening
- April 30, 2007: Gave NSERL tour to Kevin McDonough - former partner of Cyrix
- April 9, 2007: Gave NSERL tour to Chris Progler - CTO of Photronix
- April 5, 2007: Gave NSERL tour to Monica Reyes from Fluor Engineering
- Feb. 3, 2007: EJS Graduate Student Recruiting Summit. Gave tours and met with potential students.
- Jan. 4, 2007: Served as adviser for EJS graduate school orientation (microelectronic devices and circuits)
- Aug. 4, 2006: Served as adviser for EJS graduate school orientation (microelectronic devices and circuits)