8B 50 MB/s Serial Input Digital to Analog Converter with Analog Comparator

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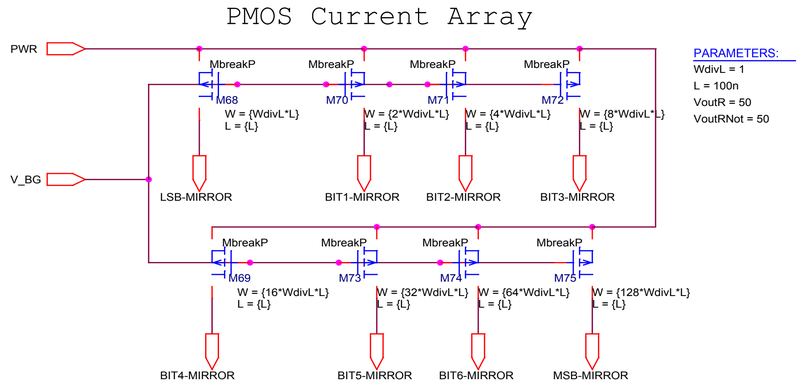
Project Goals:

- Obtain Serial Input Data
- Select 8-bits of Data and Pass to DAC at a Speed of 50 MHz
- Obtain Stable Input Voltage Source for DAC
- Design a Power on Reset
- Compare DAC Output Voltage to Reference Voltage
- Achieve Near-Linear Quantized DAC Output Voltage
- Achieve Low Power Consumption
- Understand Deviations from Ideal Components
- Interpret Graphs and Modify Parts Accordingly
- Troubleshoot Unexpected Results

Project Overview:

- Research and Design
  - Determine what component blocks are needed
  - Select the type of circuit appropriate to each block
- Proposal
  - Choose the kind of DAC that will work best for this project
  - Split up responsibilities for the assembly and testing of each block
- General Assembly
  - Define and test simple separate blocks with ideal components
  - Use as many electronics packages (op-amps, counters, voltage supplies) to facilitate quick circuit implementation
  - Troubleshoot inconsistencies
- Implement Full Circuit
  - Assemble all blocks to form one large circuit
  - Create separate but connected schematics for major parts
  - Replace electronic packages with component-level schematics
  - Notice significant differences from ideal components and select additional components to compensate as necessary
  - Increasing level of circuit complexity increases possibilities for assembly error

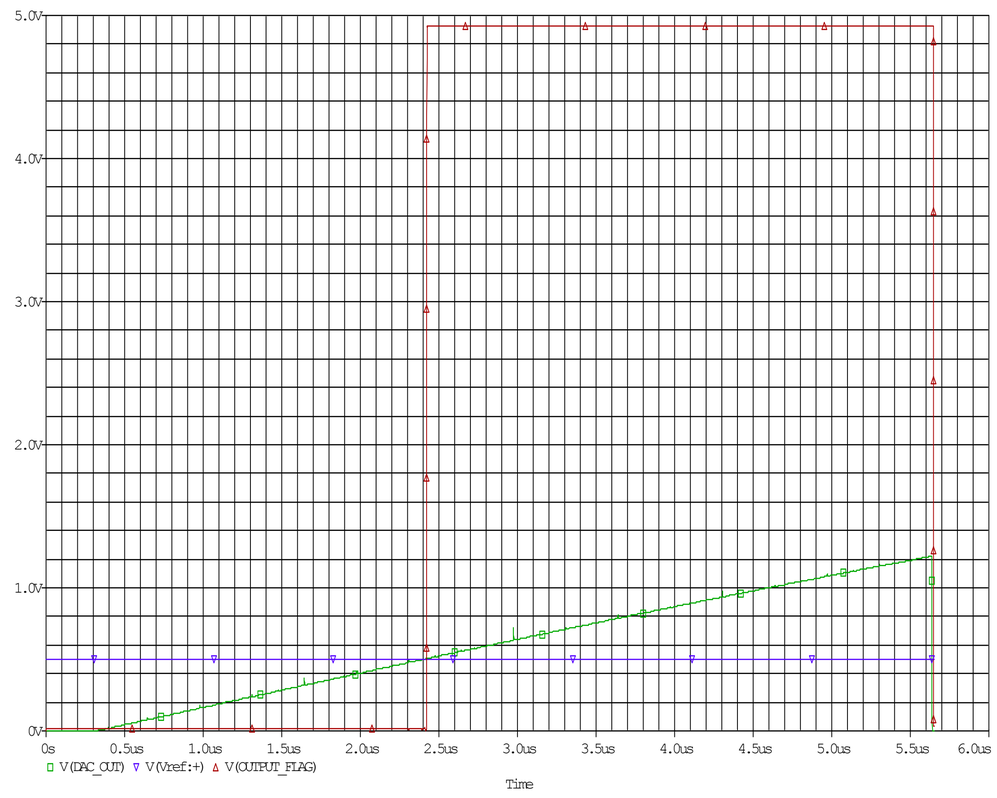
PMOS Current Array



PMOS Current Output Switches

Project Results:

- The DAC runs at 48.1 MHz instead of 50 MHz due to software limitations
- Power consumption 5 W
- Vref = .5 Vdc
- Vbias = 1.239V
- Vt = 0.026 eV
- Minimum length 100nm
- Minimum width 90 nm
- Vdd Max = 25 Vdc
- Temperature sweep from -40°C to 80°C = Vbias change of .04V
- INLmin = 0
- INLmax = 5.87 LSB



Project Conclusions/Outcomes:

- Used multiple instances of modified band gap circuit
  - Simulated other voltage supplies
  - Decided not to use these circuits; circuits were very time-consuming to design
  - Decided on instance of band gap with additional hardware to produce desired voltage for DAC current mirrors
- Implementations that did not work
  - Both the MOS and BJT op amp models worked ideally with no load. Decided to add another opamp to boost band gap voltage
- PMOS current array and current output switches are more ideal for architecture than NMOS
- Binary weighted DAC was not practical and a current steering architecture was more ideal