

VENKATESH ACHARYA

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OBJECTIVE

To work with the best company and to contribute my maximum in their challenging product development in Analog/Mixed Signal/RF Integrated Circuits.

EDUCATION

Currently enrolled for Ph.D. Aug 2005 -

University of Texas at Dallas, Richardson TX, GPA 4.0/4.0

Research Topic: Low voltage, Low Power, High speed Data Converters

Adviser: Prof. TR Viswanathan, Research Professor, UTD

Master of Technology, Electrical Engineering 2002 – 2004

Indian Institute of Technology Madras, Chennai, GPA 3.6/4.0

Dissertation: Design and Implementation of CODEC for Audio Signal Applications.

Adviser: Dr. Vinita Vasudevan, Assistant professor, IITM

Bachelor of Engineering, Electrical and Electronics Engineering, 1998 – 2002

National Institute of Technology Karnataka, Surathkal, formerly Karnataka Regional Engineering College, Surathkal GPA 4.0/4.0

TEACHING EXPERIENCE

Department of Electrical Engineering, University of Texas at Dallas Aug 2005 - Date

Teaching Assistant for Advance Analog Circuits, Advanced Analog IC Design, Advanced Analog System Design, RF and Microwave Communication Circuits and Instrumentation Lab.

Department of Electrical Engineering, Indian Institute of Technology, Madras India July 2002 - May 2005

Teaching Assistant for Electrical Circuits(Undergraduate course), Analog and Digital Circuits Lab, Instrumentation Lab

PROFESSIONAL EXPERIENCE

Sanyo LSI Technology Pvt India Ltd, Bangalore, India, May 2004 - July 2005

Design Engineer, Analog Group

Projects

- Analog Multiplier** : Gilbert-cell based design using 0.18 μ TSMC Process for Wattmeter Applications
- Ring Oscillator** : 10 Mhz Ring oscillator is designed using replica biased differential delay element with 0.18 μ TSMC Process. This design is based on work by Process and temperature compensated CMOS voltage-controlled oscillator for clock generators by Lee S S, Kin S W. This design has been tested successfully on silicon.
- Bandgap reference** : Curvature compensated Bandgap reference using 0.6 μ Sanyo Process. This design is designed using all BJTs.
- Class AB Power Amplifier** : 250 mW class AB Power Amplifier is designed using 0.15 μ GSMC Process. This design is based on "Large-Swing CMOS Buffer Amplifier" by K Nagaraj. This design has been tested successfully on silicon.
- Class D Power Amplifier** : Class D Power Amplifier capable of delivering 600mW is designed using 0.15 μ GSMC Process. This design is under fabrication.

PUBLICATION

1. Acharya Venkatesh, Kakde Sandip, Tantry Shashishar *Design and Implementation of Class AB CMOS Power Amplifier using 0.15 μ GSMC Process* 9th IEEE VLSI Design and Test Symposium 2005.

COURSEWORK

Analog IC Design, VLSI Design, RFIC Design, Active/Passive Filter Design, VLSI Data Converters and Noise in Electronic Circuits.

Digital Integrated Circuit Design, Signal Processing and Computer Architecture.

Semiconductor Device Modelling, Advanced MOS Device Modelling, Compound Semiconductors, Power Semiconductors.

Advanced Analog Circuit Design, Design automation of VLSI Systems.

Advanced Digital Logic, Advanced Analog System Design, Power Management Circuits.

SKILLS

Proficient in verilog, MATLAB, Scilab

Familiar with VHDL, Orcad

CAD tools from Cadence, Synopsys, Tanner and Xilinx; Magic, HSpice, PSpice, Modelsim, Symplify

ACHIEVEMENTS And ACTIVITIES

Secured 2nd rank in B.E. in Mangalore University.

Secured 2nd rank in Mathematical Talent Search Examination.

Secured a percentile of 99.8% in GATE 2002, Electrical and Electronics.

Recieved prestigious award by Dr. T.M.A. Pai group, Manipal, *Udayavani Datti Prashasthi* during 1997-98 for excellence in in Pre-University

Passed with Distinction in JLPT(Japanese Language Proficiency Test) Level4 in Dec 2004.

REFERENCES

1. Prof. T R Viswanathan tr.viswanathan@utdallas.edu
Research Professor, University Of Texas at Dallas
2. Dr. Jim Hellums hellums@utdallas.edu
Professor, University of Texas at Dallas
3. Dr. Shanthi Pavan shanthi@ee.iitm.ac.in
Assistant Professor, Indian Institute of Technology, Madras