Digital Logic and Computer Design
UTD CS 4341
Fall 2008
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Class room overviews and announcements

This file will be updated as classes progress

Class 1. Monday, Aug. 25, 2008

- Course organization
- Objectives
- Topics to be taught in the course

Course website

- Main course website directory is
  - www.utdallas.edu/∼datta/CS4341/fa08
  - It contains this class overviews pages and the syllabus page
- This site has additional directories
  - notes
  - exams
    - After midterm exams, solutions will be posted here
  - HWsolns
    - Homework solutions will be posted here
  - project
    - Project handouts, upgrades, etc. will go here

Boolean Algebra and Logic Circuits

- Definition of a Boolean variable
- Definition of a Boolean function of many variables
- Elementary Boolean operations
- Logic gates
- Multiple input extensions of operations and gates
- Logic circuits for Boolean expressions
- Identities
- Boolean algebraic simplification

Class 2. Wednesday August 27, 2008

Topics of the last class

- Course organization, objectives, topics
- Boolean Algebra and a little on simplification

Topics for today

- Boolean algebraic simplification
- Boolean functions in general
- Algebraic expression for every Boolean function
- Minterm, Sum of minterms
- Product term or implicant
- Sum of Products form
- Karnaugh maps

Announcement

- HW 1: Questions 2.7 and 2.9 (a) and 2.9 (b) in the text book
  - Due Wednesday Sept. 3, 2008
- Helpful hints to navigate through the text book
  - We are discussing Chapter 2
  - We will deal with gates and circuits designed from gates
  - We will not study internal details of gates
  - We will acknowledge that practical gates have delays. But we will not study details of delays
  - For exams, I do not expect you to remember the names of the identity properties. De Morgan's theorem is an exception!

Important points on Boolean functions and K-maps

- A minterm is the AND operation of every variable in the domain, each variable appearing exactly once, with or without a complement
- A minterm is obviously a Boolean function. The truth table for a minterm has exactly one entry mapping to Boolean 1. All other entries map to Boolean 0
- Every Boolean function can be represented as " 0, a single minterm, or the OR operation of two or more minterms" Such form of Boolean expression is called the "Sum of Minterms" form
- Therefore, every Boolean function can be expressed as a Boolean expression
- A product term is the AND operation of 1 and zero or

more variables in the domain, each variable appearing exactly once, with or without a complement

- As a consequence, we see that every minterm is a product term. But every product term is not a minterm.
- As a consequence, a Boolean 1 is a product term
- The expression 0, a single product term, or the OR operation of two or more product terms is called the "Sum of Products" form
- Every Boolean function has at least one Sum of Products form Boolean expression for it. This is true since every Sum of minterms expression is also a Sum of Products form
- In general, there are many Sum of Products forms for a

Boolean function. We are interested in "simpler ones" among these. Therefore, we define a criterion to evaluate the complexity of a Sum of Products form, as follows.

- A literal in a Sum of Products form is every occurrence of every variable
- The complexity or cost of a Sum of Products form is defined as the total number of literals in a Sum of Products form
- We can now state an optimization problem: Among all possible Sum of Products forms for a Boolean function, find one that has the least possible number of literals in it.
- This problem is easy to solve for Boolean functions

made of upto 4 Boolean variables, with the use of a Karnaugh map (or a K-map).

- A product term is also called an implicant since, if a product term of a function maps to 1, for a particular combination of input values, the entire function also maps to 1 for that input combination (implication)
- If a product term (or an implicant) of a function cannot be combined with any other minterm not covered by that product term, we call it a "Prime Implicant." Therefore, a Prime Implicant on a K-map cannot be expanded to include any additional 1 on the K-map.
- If a Prime Implicant of a function covers a 1 not covered by any other Prime Implicants of the function, the Prime Implicant in question (the former) is called an "Essential Prime Implicant"

- A consequence: Every Essential Prime Implicant of a function must be present in a minimized Sum of Products form of the function

Class 3. Wednesday, September 3, 2008

Topics studied in the last class

- Algebraic simplification of Boolean expressions
- Boolean functions
- Every function has at least one Boolean expression
- SOP (Sum of Products form)
- K-map structure, adjacency, Product terms from K-maps

Topics for today

- Prime Implicant
- Essential Prime Implicant (EPI)
- K-map minimization examples
- Don't care entries

Announcement

- Website split for two sections. Terminology is clear
- HW submission: Handwritten (legible and clear) on paper. Staple or otherwise fasten multiple sheets. Clearly write your name HW number, and date.
- HW 2: Solve HW 1 questions using K-maps
- Due Monday September 8
- Blank K-maps posted for your convenience

Class 4. Monday September 8, 2008

Topics studied in the last class

- Essential Prime Implicants
- K-map examples
  - In some cases, we may need to carefully consider some alternative sets of PIs to cover the function and choose the set with the least number of literals

Topics for today

- More K-map examples
- Don't care entries and their use in minimization
- A different Boolean algebraic representation for Boolean functions
- Maxterm, product of maxterms
- Sumterm, Product of Sums (POS)
- Every Boolean function has at least one POS form
- K-map minimization of POS forms
  - Reverse the roles of zeros and ones on the K-map
  - That is, deal with the complement of the given function to begin with
  - Minimize the SOP of the complement of the given

function

  - Express the given Boolean function as the complement of a minimized SOP
  - Apply DeMorgan's theorem

- Proof that we do get the *minimized* POS by this method
- K-map examples of POS, with don't care entries
- Examples of logic circuits

Announcement

- TA information is announced in the updated syllabus file
  - TA' name: David Perkins
  - His email: dpp074000@utdallas.edu
  - His office: ECSS 4.229
  - His office hours: Mondays 6:50 - 7:50 PM and Wednesdays 1:25 - 2:25 PM
- Lots of Boolean functions as 4×4 arrays are posted in a file called kmapfns.pdf
- These are additional K-map examples for you

Definitions and consequences related to POS forms

- A maxterm is the OR operation of every variable in the domain, each variable appearing exactly once, with or without a complement
- A maxterm is obviously a Boolean function. The truth table for a maxterm has exactly one entry mapping to Boolean 0. All other entries map to Boolean 1
- Every Boolean function can be represented as "1, a single maxterm, or the AND operation of two or more maxterms" Such a form of Boolean expression is called the "product of maxterms" form
- Therefore, every Boolean function can be expressed in a product of maxterms form.
- A sum term is the OR operation of 0 and zero or more

variables in the domain, each variable appearing exactly once, with or without a complement

- As a consequence, we see that every maxterm is a sum term. But every sum term is not a maxterm.
- As a consequence, a Boolean 0 is a sum term
- The expression 1, a single sum term, or the AND operation of two or more sum terms is called the "Product of Sums" form
- Every Boolean function has at least one Product of Sums form Boolean expression for it. This is true since every Product of maxterms expression is also a Product of Sums form
- In general, there are many Product of Sums forms for a Boolean function. We are interested in "simpler ones"

among these. We already have a criterion to evaluate the complexity of a Product of Sums form: the total number of literals in the POS.

- We can now state an optimization problem: Among all possible Product of Sums forms for a Boolean function, find one that has the least possible number of literals in it.

Class 5. Wednesday Sept. 10, 2008

Topics studied in the last class

- Don't care entries in truth tables and their use in minimizing SOP forms
- Maxterm, sum term, Product of Sums (POS) expressions for Boolean functions
- K-map minimization of POS expressions

Topics for today

- Proof that the method does minimize POS forms
- POS minimization examples including don't care entries
- Logic circuits

Announcement

- Solutions for HW 1 and 2 posted
- HW 3: Questions 2.4 and 2.8 in the text book. Due date: Wednesday Sept. 17, 2008
- Midterm 1 is on Monday Sept. 29
- Therefore, we should decide on the first additional review class soon.

Class 6. Monday Sept. 15, 2008

Topics studied in the last class

- Completion of minimization of POS forms – with don't care entries too
- Entering a function on a K-map
- Logic circuits – various forms
  - Any expression to circuit (with only horizontal and vertical lines)
  - Two level AND-OR circuits (requirement of NOT gates is taken for granted)
  - Two level NAND-NAND
  - Two level NOR-NOR
- Decoder building block

– without and with control enable terminal

Topics for today

- Decoder expansion
- Multiplexer
- ROM and PLA
- Sequential logic design

Announcement

- Notes on Sequential logic and circuits posted on the website
- First review class for the afternoon section 002: Friday, Sept. 26, 3:00 - 4:15 PM in classroom ECSS 2.201
- Material from the text book we did not study:
  - Sections 2.5, 2.6, and 2.9
- Initial discussion about project: A common project or different group projects?

Class 7. Wednesday Sept. 17, 2008

Topics studied in the last class

- Discussion of possible projects
- Tristate buffer
- Multiplexer

Topics for this class

- ROM and PLA
- Sequential logic and circuits
  - Analysis of NAND latch
  - Clocking gates and clocking
  - Master slave SR flip-flop
  - Master slave D flip flop

Announcement

- Review class for section 002: Friday, Sept. 26, 3:00 - 4:15 PM in classroom ECSS 2.201 – confirmed
- I will teach Arithmetic Circuits after Sequential circuits, following the organization of the text book
- CS 4141 Laboratory
  - There are two sections: 001 (9:30 - 11:20 AM) and 002 (12:30 - 2:20 PM)
  - My TA David and I handle section 002
  - Dr. Bhowmik and her TA handle section 001
  - Section 001 sessions have already started (I am told)
  - Section 002 is starting this week
    - No need to prepare for the first lab; just show up

Possible projects

1. Development of algorithm and program for minimization of SOP forms for k variables, $k > 4$
2. Sequential multiplier – algorithm and circuit design
3. Combinational multiplier – method and circuit design
4. Development of the architecture for a very simple computer – complete external specification; instruction set and instruction formats
5. Development of the datapath for the simple computer
6. Development of single cycle control unit for the simple computer
7. Other project/s you like – discuss with me
8. Development of nice circuit diagrams for well specified

combinational and sequential logic functions – output in xfig or .eps form – anybody?

9. Development of algorithms and programs for algebraic simplification and output in latex format
10. K-map generation with color coded PI grouping for minimization. For example, green for EPI, yellow for other PIS to make up minimized SOP, and red for PIs unused in minimized SOP
11. A common individual project – specifications being developed by me
12. Absolute deadline – Monday, November 17, BEFORE class

Class 8. Monday, Sept. 22, 2008

Topics studied in the last class

- ROM and PLA
- Sequential logic and circuits
  - Analysis of NAND latch

Topics for today

- Clocking gates
- Master-slave SR flip-flop
- D flip-flop
- Definition of a synchronous sequential machine
- Analysis – Logic circuit to state table

No particular announcement today

Class 9. Wednesday, Sept. 24, 2008

Topics studied in the last class

- Clocking gates
- Master-slave SR flip-flop
- D flip-flop
- Definition of a synchronous sequential machine
- Example of a machine
  - Specified with Boolean equations
  - Specified as a logic diagram

Topics for today

- Analysis – development of state table from logic diagram
- Another form of representation for a machine – State diagram
- Tracing the state and output sequence given an initial state and an input sequence

Announcement

- The Corrected version of the pdf file in the notes directory, `pt03_sequential.pdf` uploaded
- Don't forget the review class on Friday, Sept. 26, 3:00 - 4:15 PM in this room – ECSS 2.201
- I will come prepared to solve some particular problems; if you suggest some problems, they take priority
- Midterm exam 1 – next Monday during class hours
- Material: Upto and including analysis of sequential circuits
- Solutions for HW 3 uploaded. Additional explanations added for HW 1 and 2 solutions

Class 11. Wednesday, Oct. 1, 2008

- We discussed and solved some problems during class 9 on Friday Sept. 26.
- Midterm 1 was held during class 10

Topics for today

- Design of synchronous sequential machines
  - Through examples
  - In this course, we will only design simple machines: The number of states is known

Announcement

- HW 4: Exercise 3.24 and 3.25 in the text book. Both problems are related. Due date: Wednesday Oct. 8, 2008
- The "common" project handout is posted
- Solutions to midterm 1 is posted
- Midterm 1 grades will be given; statistics not available yet

Class 12. Wednesday, Oct. 6, 2008

Topics studied in the last class

- Design of sequential machines

Topics for today

- Digital Building blocks – larger systems than elementary building blocks such as decoders and multiplexers
- This material is from Chapter 5 of the textbook
- We will cover only the following subtopics in the book
  - Arithmetic circuits based on Ripple Carry Adder only
    - No Carry Look Ahead adders
    - No prefix adder
    - No delay calculations
  - Various arithmetic operations and controlling them
    - Operations in 2's complement notation
    - Negation, subtraction, comparisons
    - Increment, decrement, wraparound count up and down

    - Multiplication and division by 2
    - No multiplication of two long words
    - No floating point operations

- Logic operations and ALU
- Shifters
  - Those that are useful for our MIPS computer only
- Memory units
  - Constructed from gates only (no MOS structures)
- Not all the above topics will be completed today

Statistics of class performance in Midterm 1 will be shown

Class 13. Wednesday, Oct. 8, 2008

Topics studied in the last class

- Quick revision of arithmetic of signed integers in 2's complement notation
- Full adder, Ripple carry adder
- Adder/subtracter

Topics for today

- Other arithmetic operations: INC, DEC, count-up, count-down
- Logic operations
- Shift operations
- ALSU

Announcement

- Any discussion on project?
- I should put a hard deadline on selection of individual projects
- Notes from previous class and a summary notes file on arithmetic uploaded
- HW 5: Due date: Wednesday Oct. 15
  - Represent (a) $A = -83$, (b) $B = 15$, (c) $C = 41$, and (d) $D = -37$, each in 2's complement notation using 8 bits (including the sign bit, of course)
  - Perform $A + C$, $A - C$, $C - A$, $D - B$, and $A + D$
  - Prove that the procedure for signed decrement also works for unsigned wrap-around count-down, if OVF is ignored (corrected after class on Oct. 8)

- Develop combinational functions for C_n, C_{n+1}, and OVF from a_n, b_n, and s_n (note the correction, s_n, in place of the original but wrong c_n) during the addition of signed integers in 2's complement notation (this part of HW was added during the class on Oct. 8).

Class 14. Monday, Oct. 13, 2008

Topics studied in the last class

- Arithmetic operations
- Structure of arithmetic unit

Topics for today

- Logic operations and logic unit
- Shift operations and shift unit
- ALSU

Announcement

- Class notes from the last class uploaded
- Deadline to select and get my OK for individual projects: Wednesday Oct. 15

Class 15. Wednesday, Oct. 15, 2008

Topics studied in the last class

- Logic and shift operations and units
- ALSU

Topics for today

- Registers
- Memory systems
  - To be developed strictly from gates
  - Basic memory cell – not a master-slave flip-flop
  - Interconnecting a rectangular array of cells for a memory chip
  - Interconnecting memory chips

Announcement

- Notes developed in the last class is uploaded
- Notes on registers and memory systems uploaded
- Brief discussion on the default project today
- HW frequency is reduced a little to allow time for project

Class 16. Monday, Oct. 20, 2008

Topics studied in the last class

- Registers
- Memory systems
  - Developed strictly from gates
  - Basic memory cell is not a master-slave flip-flop
  - Interconnecting a rectangular array of cells for a memory chip

Topics for today

- Interconnection of memory chips to realize a larger memory system
- Input-output port
  - One chip in a memory system may be an I/O port chip
  - Needs two sets of address input lines, one set for computer and one set for outside I/O devices
  - Similarly, two sets of data lines
  - Both sides should be able to read all the time
  - Both sides should be able to write all the time, even into the same word, without any physical destruction
    * The exact bit pattern written into the memory

word is unpredictable in such a case

  - In practice conventions are used to design software so that each side knows whose turn it is to write

- Bus transfer system – data movement subsystem of the datapath

Announcement

- Additional pages added to the current notes pdf file
- Solutions for HW 4 updated and for HW5 uploaded
- Midterm 2 is on Monday November 3
- Review class: We could have two review classes in which I will solve design problems related to Midterm 2
- When should we have them? 1:30 - 4:15 PM with a break of 15 minutes on Friday October 31?
- Or, one this Friday and one next Friday?

Class 17. Wednesday, Oct. 22, 2008

Topics studied in the last class

- Interconnection of memory chips to realize a larger memory system
- Input-output port
- Bus transfer system – data movement subsystem of the datapath

Topics for today

- Datapath, microoperations, and control

Announcement

- Notes on today's material posted as `pt05_datapath_microp081022.pdf`
- Upcoming review classes before Midterm 2
  - Friday October 24, 3:00 - 4:15 PM
  - Note the room – GR 4.428
  - This is in the Green (no, not the color) building, at the other end of the campus
  - I will solve design problems from Midterm 2 material
  - If you suggest problems or have questions, they take priority

Class 18. Monday, Oct. 27, 2008

Topics studied in the last class

- Datapath, micropoperations, and control word

The second review class was held on Friday Oct. 24. Problems based on Midterm 2 material were solved. Notes (corrected) are uploaded on the course website.

Topics for today

- Review of MIPS instructions

Announcement

- Review class 3. This Friday October 30, 3:00 - 4:15 PM in our classroom
- MIPS instructions and some hardware schematics from the book are posted as file `pt10_examhandout.pdf` in the notes directory
- Slides on Chapter 7 from the textbook author uploaded as file `pt07_DDCA_Ch7.ppt` in the notes directory
- MIPS machine design class notes uploaded as file `pt07_a_MIPS_design.pdf`

Class 19. Wednesday, Oct. 29, 2008

Topics studied in the last regular class

- General principles and differences in Datapath and Computer
  - Computer: machine that can execute a machine language program stored in its RAM
  - Machine instruction set: specifies the computer
  - General Datapath: can execute a predesigned set of microoperations, usually one microoperation during a clock period
  - Specially designed datapaths, for particular applications, may execute multiple microoperations at a time
- Review of MIPS instructions

- Related hardware considerations to implement MIPS, hand in hand.

During our 2nd review class on Friday Oct. 24, we solved some problems

Topics for today

- Continue with MIPS instructions and hardware requirements

Announcement

- Review class 3: Friday Oct. 31, 3:00 - 4:15 PM in ECSS 2.201
- Midterm 2: Coming Monday, November 3, during class hours
- Material: Starting from Design of sequential machines up to all topics to be covered today
- I will be traveling on Sunday. Our TA David Perkins and my PhD student Ajay Kulkarni will proctor the midterm. They will not provide any clarifications on questions. Do your best – same rule for all students
- I will be on travel and WILL NOT hold classes on Wednesday November 5

Class 21. Monday, Nov. 10, 2008

We had midterm 2 during the 20th class on Nov. 3. We had review class 3 on Friday Oct. 31. Topics studied in the last regular class

- Overall hardware for single cycle MIPS machine

Topics for today

- More details on how the book develops facilities around the datapath for single cycle MIPS machine

Announcement

- Midterm grades will be distributed
- Statistics not available yet

Class 22. Wednesday, Nov. 12, 2008

Topics studied in the last class

- Some details of MIPS machine hardware requirements and their corresponding realizations

Topics for today

- Continue with more of the same

Announcement

- Midterm 2 performance statistics will be shown
- Midterm 3 will be held during class hour and in this class room on Wednesday, November 26, 2008
- Material: MIPS computer hardware and related
- No other final exam

Class 23, Monday November 17, 2008

- Topics studied in the last class
  - Various aspects of the design of MIPS machine
- Topics for today
  - Continue with the same and make conclusions on the general structure of the control circuits
- I am introducing a 7-bit bit pattern called the MOPCODE. This is the modified OPCODE. It has one bit specifying whether the instruction is a register type or not. The rest of the bits are funct if it is a register type instruction. They are the OPCODE bits if the instruction is not a register type instruction. Therefore, this 7 bit MOPCODE determines the type of the instruction and the nature of the operation.

Announcement

HW 6: Answer the following questions about the single cycle MIPS machine. Due date: Monday November 24.

1. How many data input buses does the Register file have? Specify a list of data sources for each of them.
2. How many registers can we simultaneously address in the register file? What are their functions? Where do these register addresses come from?
3. How many different data words can the register file simultaneously produce? What are the different purposes of these outputs?
4. List the different sources for each data input to the ALU.
5. List the different sources for the address input to the

RAM.

6. List the different sources for the data input to the RAM.
7. List the different destinations to which the data output from the RAM needs to reach.
8. How many different places does the input for the PC (Program counter) come from? What are they? What are their functions?

Class 24, Wednesday November 19, 2008

- Topic studied in the last class
  - Various aspects of designing the control circuits for MIPS machine
- Topic for today
  - We will consolidate all the control requirements and corresponding circuits
- No particular announcement today

Class 25, Monday November 24, 2008

- We have completed the final design of the single cycle MIPS machine and its control unit.
- Today, we will have questions and answers type of review
- Including the 3 completed additional review classes, the present class will complete 28 classes.
- Midterm 3 is on Wednesday November 26 during the class time period
  - Material: Design of single cycle MIPS machine
  - additional handout will be provided, as discussed in class
- HW 6 solutions will be posted after this class