

**Fall 2008; CS 4341.501, Digital Logic and Computer Design
and Laboratory CS4141**

Class Mondays and Wednesdays 5:30 - 6:45 PM in ECSS 2.305

Instructor G. R. Dattatreya

Office: ECSS 4.208

Office Hours: Mondays and Wednesdays 3:50 - 4:50 PM

Additional hours by appointment

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TA David Perkins

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Office: ECSS 4.229

Office Hours: Mondays 6:50 - 7:50 PM and Wednesdays 1:25 - 2:25 PM

Text Book David M. Harris and Sarah L. Harris, *Digital Design and Computer Architecture*. Morgan Kaufmann Publishers, 2007

Evaluation Exam 1: 25%; Monday Sept. 29, 2008; 5:30 - 6:45 PM; class room
Exam 2: 25%; Monday Nov. 3, 2008; 5:30 - 6:45 PM, class room
Exam 3: 25%; Monday Dec. 8, 2008; 5:30 - 6:45 PM, class room; not comprehensive
Design Project: 15%
Home work: 10%

Objectives To study topics leading to the understanding and ability to design a computer,

Topics Topic 0: Fixed point arithmetic in 2's complement notation: Notation, weighted sum, range, negation, addition, subtraction, multiplication and division by 2.

Topic 1: Boolean algebra and logic circuits: Simplification including K maps
Combinational circuits including NAND, NOR, ROM, and PLA realizations.

Topic 2: Combinational building blocks: Full adder, Ripple Carry Adder, 2's complement adder and overflow detection circuits. Unsigned wraparound increment and decrement. Tristate buffer. Decoder (with and without enable), Multiplexer.

Topic 3: ALSU design: Implementation of arithmetic, logic, and shift operations. Multiplexing them and implementing them in one functional block with two input operands with carry-in, one output operand, and status flag outputs.

Topic 4: Sequential circuits and registers: Analysis of a NAND/NOR latch. Design of a fully synchronous flip-flop. Definition and Analysis of synchronous

sequential circuits. Design of simple sequential circuits (simple implies outputs = state variables; that is, no state minimization). Registers.

Topic 5: Data transfer bus design: Register file. Uni- and bi-directional buses. Interaction of a functional block with multiple buses.

Topic 6: Memory unit design: Basic Binary cell with Read, Write, Select, and Tristate Output lines. Binary cell with two sets of input and output lines for memory mapped I/O RAM chip design RAM chip interconnections Complete memory unit with bootstrap loader ROM and memory mapped I/O ports.

Topic 7: Computer cycles: Parts of a machine instruction: Instruction Fetch, Operand Fetch, Execute OP CODE, Status flags. Store result, Check interrupt. Microoperations for fetch, for various addressing modes, stack operations, and interrupt check.

Topic 8: Control unit design.

Topic 9: Input/Output interface: Program controlled and interrupt initiated I/O Interface to handle multiple interrupts Direct memory access (as time permits)

Prerequisites Prerequisite: CS 3340 and PHY 2326. Corequisite: CS 4141

The following topics are assumed to be known to students:

1. Representation of positive integers by Binary, Octal, and Hexadecimal numbers.
2. Representation of signed integers in sign-magnitude and 2's complement notation.
3. Addition and subtraction of positive binary integers.
4. Boolean variables and Boolean operations.

CS4141 The accompanying laboratory, CS 4141 will start a few weeks after the semester starts. The instructor will announce the details in the class.

Important Students should be aware of academic dishonesty policies and abide by it. All HW, project, and of course, the exams, are required to be of "individual efforts."