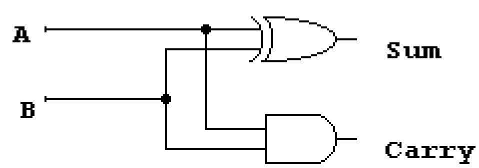
The University of Texas at Dallas
Electrical Engineering Department
EE 2110: Beginning Digital Logic and Computer System Fundamentals
Experiment #2 – Digital Adder Circuits

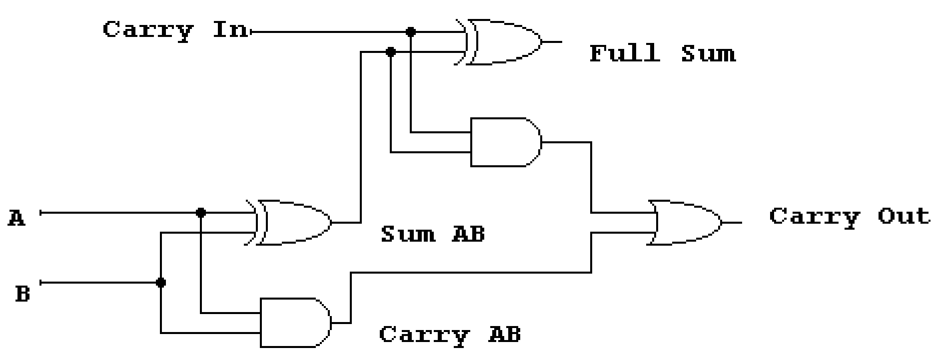
1. **Introduction:** In the previous laboratory exercise, we studied combinational logic circuits. Today we will study the combinational logic adder circuit. While arithmetic circuits such as the digital adder circuit are almost always used in sequential digital systems (typically microprocessor or computer processing subsystems), they are, in fact completely combinational logic in the way they are constructed. The "sequential" aspect of their operation is in the way the operands (numbers to be added or otherwise manipulated) are gated into the processing elements, and the way in which the result is stored after the operation. Today our concern will be strictly with the combinational logic of the digital addition function.

2. **Goal of this exercise:** The purpose of this lab is to familiarize students with the functionality of the digital adder circuit. We will operate the 74LS83 4-bit full adder to get the feel of the adder operation. We will then build and operate a 2-bit full adder from basic combinational 74LS logic.

   Theory of experiment: We have recently studied the adder in class. We know that the basic "half adder" adds two bits to produce an arithmetic result and a possible carry. The basic diagram of the half-adder is:



This circuit produces a 1 sum whenever A or B is 1, otherwise "Sum" is 0. However, when both A and B are 1 (and thereby Sum is 0), Carry is 1. This circuit produces a "complete" add function as long as there is no "carry-in," i.e., as long as only two one-bit numbers are being added. If the numbers have more than one bit magnitude, however, all but the least-significant-bit (LSB) additions must have a carry-in, since there is the possibility of a carry being generated from addition of less significant bits in the number. In that case, the so-called "full adder" must be used:



The full adder contains circuitry to accommodate a carry-in from addition of the two next least significant bits. Thus, addition of the two LSBs of two numbers can be made using half-adders, but full adders must be used to add the other bits of the two numbers.

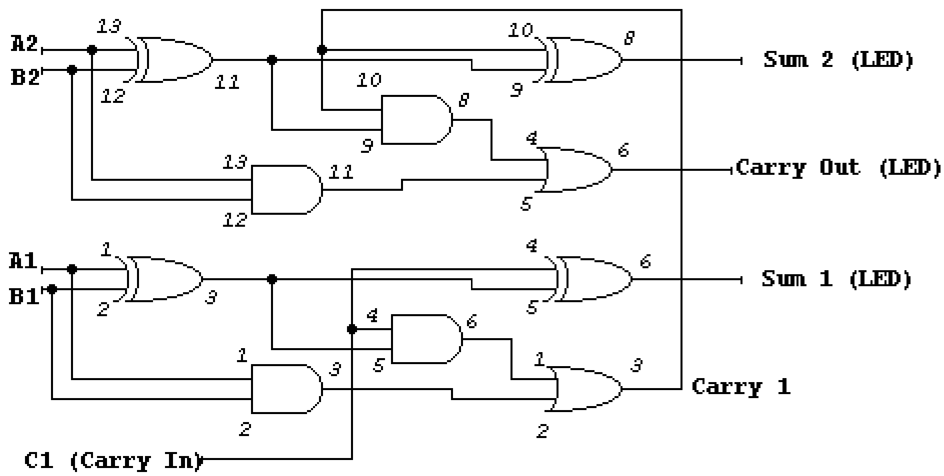
3. **Experimental Equipment List:** The following components are required for this experimental procedure:

- **IDL-800 Digital Lab. Circuits Evaluator ("breadboard" unit with test equipment and power supply built in)**
- **IDL-800 User Manual (as required)**
- **SN 74LS83 Full Adder (digital logic kit)**
- **SN 74LS08 Quad 2-input AND gate (digital logic kit)**
- **SN 74LS32 Quad 2-input OR gate (digital logic kit)**
- **SN 74LS86 Quad 2-input XOR gate (digital logic kit)**
- **Breadboard wire connection kit**
- **Pin assignment diagrams for circuits noted above (see back of this exercise outline)**

4. **Pre-Work:** Study the class notes on digital addition and study the architecture sections of half- and full-adders (Tokheim, Chapter 8).

5. **Experimental Procedure:**
   1) **4-Bit Addition with 74LS83:**
      - **Make sure power is off.**
      - **Locate the 74LS83 4-bit adder and plug it into the prototype board. Note: for all the following instructions on connections of circuits (except power and ground), please refer to the appropriate chip diagram on the last page of these instructions. Connect pin 12 to ground and pin 5 to +5V (note the difference in these power pins from the connections you used last week). Connect the parallel output sum pins (S0-S3) to LED indicators. Connect the 8 data switches to the 8 data inputs. Make sure that you connect them in an easy-to-use order, such as switch 1-A0, switch 2-B0, switch 3-A1, etc., or switches 1-4 to A0-3 and 5-8 to B0-3. Connect Carry In (denoted CI) to one of the pulse switches, and Carry Out (denoted CO) to the 5th LED input.**
      - **Make sure all the data switches are on 0. Turn on the power. Turn on the LSB A bit (A0) and note that the appropriate S bit (S0) LED lights up. Now turn on the LSB B bit (B0). Note that S0 goes out and S1 lights up. Activate the pulse switch (hold it on) and note that since this makes carry-in 1, the S0 bit lights again. With carry-in a 1, you can turn either A0 or B0 to 0, and carry-in and the other bit will still properly add to 2 (LED S0 off, LED S1 on).**
      - **Repeat this procedure with all the bits until you are familiar with the adder operation. Note that with the highest bits both added, the carry-out LED is also lit.**
      - **Turn off the power and disconnect the circuit connections.**
   2) **Constructing a 2-bit full-adder:**
      - **Constructing a 2-bit full adder will require XOR, OR, and AND gates. Obtain a 74LS86 XOR chip, one 74LS32 OR chip, and a 74LS08 AND chip from the logic parts kit. Plug them into the board. Remember: DO NOT PLUG IN TWO LOGIC CHIPS ACROSS FROM EACH OTHER ON ADJACENT VALLEYS! <u>YOU AUTOMATICALLY CONNECT ALL ADJACENT PINS TO EACH OTHER WHEN YOU DO THIS</u>.**
      - **The gates should be connected as follows (make sure power is off at this point):**

(See Next Page)



- **ALSO REMEMBER TO CONECT POWER INPUTS TO EACH CHIP!**
- **Note that the XOR, AND, and OR gate make up the full adder circuit for each of the two bits. Inputs A1-A2 (number 1) and B1-B2 (number 2) should be connected to four of the data switches. A fifth data switch should be connected to Carry In. Note that A1 and B1 are the LSBs of the numbers, and A2 and B2 the MSBs. The Sum 1-2 and Carry Out should go to three adjacent LED inputs. Make sure that all switches are in the low (0) position.**
- **Check all connections and then turn on the power. Turn on A1 and note Sum 1 light up. Now turn on B1 and note that Sum 1 goes off but Sum 2 goes on. This means that the carry (Carry 1) has propagated to the Bit 2 sum and made the output of the adder binary 2. Turn on the A2 and B2 switches and note that Carry Out now turns on (since the two 2s being added make a sum of 4, and our adder only has a 2-bit sum output, which can only show a maximum of 3).**
- **Experiment with the adder until you are comfortable with it. Then complete the following additions, noting what sum lights are on, and whether the Carry Out light is on: 1+2, 0+2, 1+2+carry, 1+1+carry, carry +3+1, carry+3+3, 2+2+carry. Tabulate your results and discuss in the project summary.**

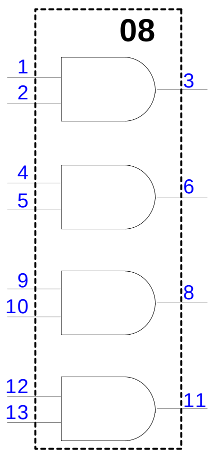
3) But can it Subtract?

- **Consider the 2-bit adder from above, with the following change: It now will be used to add and subtract numbers. Using the information provided in Lecture #4, redesign the adder to add or subtract two positive 2-bit numbers and provide the proper sign as required. For this exercise, assume that there is no "carry in" to the least significant of the two bits, so that the LSB carry-in may be used to help construct the subtract function. Have the TA verify your circuit functionality.**

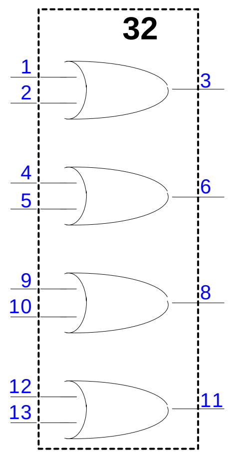
6. **Equipment Disassembly:** The experimental procedure is complete. Please disassemble the circuit wiring and replace in the wiring kit box. Check with your laboratory TA – he or she may ask you to return the wire and parts kits to the cabinet or leave them on your workbench for a following class. Make sure that your workbench is clean before leaving the lab.

7. **Laboratory Report:** As usual, please follow the laboratory report form. In your write-up, discuss the operation of the circuits and the verification of the function of each. Also include the following items:
   - **Discuss your experience in the laboratory and any problems with the procedure.**
   - **Make a drawing for a 1-bit full adder without using an XOR gate. How much more complicated is this adder?**
   - **Show the truth table of the 2-bit adder for the cases listed in part 2 of Section 5.**
   - **Make a drawing of the 2-bit adder/subtractor you designed in part 3 of Section 5.**
   - **Discuss any insights gained from the exercises.**

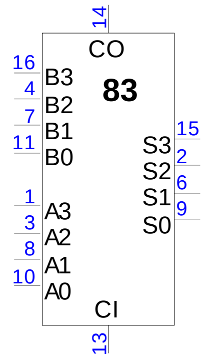
8. Circuit Diagrams: Here are the pin-outs for the circuit elements used in this laboratory:



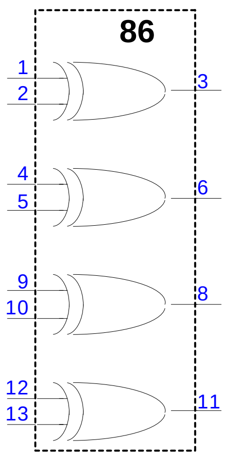
SN 74LS08 Quad 2-input AND gate



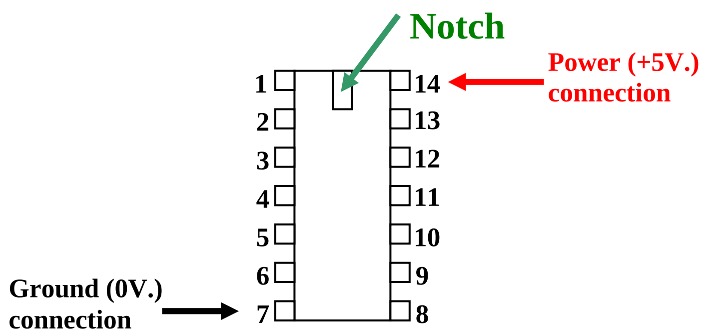
SN 74LS32 Quad 2-input OR gate



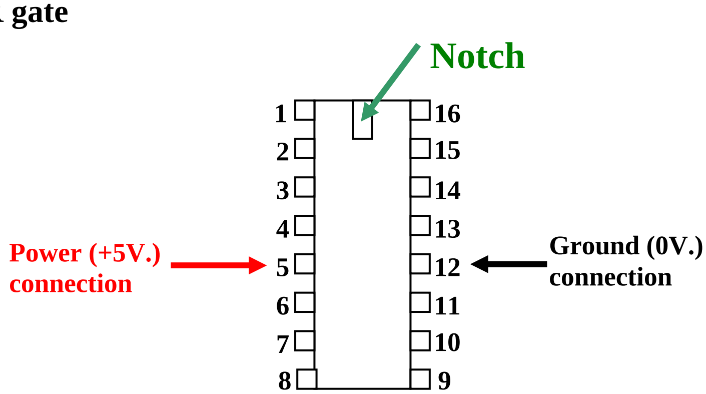
SN 74LS83 4-bit full adder



SN 74LS86 Quad 2-input XOR gate



74 LS XXX Outline for all chips but 74LS83



Physical chip outline for 74LS83