

The University of Texas at Dallas
Electrical Engineering Department
EE 2110: Beginning Digital Logic and Computer System Fundamentals
Experiment #3 – Familiarization with Bistable Circuits (Flip-Flops or Latches)
and Basic Sequential Circuits

- 1. Introduction:** In laboratory exercises 1 and 2, we became familiar with the logic gates which represent the six fundamental Boolean functions (NAND/AND, NOR/OR, XOR, and NOT) and with binary adder circuits. In this laboratory we will study another type of logic function that we have discussed in class – the bistable multivibrator, or flip-flop. Simple logic gates, such as we have studied so far, are referred to as combinational logic. Such logic circuits have outputs that depend only on their inputs. Thus, the output of a combinational logic circuit changes state as soon as the input stimulus is changed. Bistable circuits, on the other hand, may maintain their internal state, under certain conditions (and so long as power is available to the circuit) even when the input stimulus is changed. Bistable circuits are representative of the class of sequential logic. We will investigate the behavior of simple bistable circuits today. We will also become familiar with two other devices which are composed of flip-flops (hereafter abbreviated FF), and which are very important subsystems in computer architecture: the shift register and the binary counter. Both devices use bistable circuits, which we have learned will maintain either of two states after being set or reset.
- 2. Goal of this exercise:** The purpose of Experiment #3 is to familiarize students with the functionality of the simple R-S flip-flop (or bistable circuit), with the operation of D and J-K flip-flops, and with the construction of a clocked flip-flop (essentially a clocked D-type FF). We will build the RS and clocked D flip-flop circuits in the lab. We will then extend these concepts to two of the most common sequential circuits, the serial-to-parallel shift register and the simple binary counter. After operating the 74LS195 shift register and the 74LS163 binary counter, we will construct very similar devices from D and J-K flip-flops on our prototype boards.
- 3. Theory of experiment:** We have studied various FF circuits in class. The basic types that we will explore today are:
 - **R-S FF (built in the lab):** Basically an asynchronous circuit whose Q output is activated high (1) by a negative pulse on the S input and whose \bar{Q} output is activated high by a negative pulse on the R input. Simultaneous low S and R inputs are forbidden (both Q states will be high).
 - **D FF:** Essentially a clocked FF with only one input; may have asynchronous Preset and Clear.
 - **J-K FF:** Similar to the clocked R-S FF, except that the circuit is wired so that simultaneous “1” inputs on J and K produce a toggle of the FF to the opposite state rather than an undefined state.
 - **Clocked D FF (built in the lab):** A variation on the clocked R-S FF in which the R input is created by inverting the S input.

In order to demonstrate the circuit mechanics of the R-S FF, we will build the circuit from a simple 74LS00 chip using NAND gates. We will then operate and observe the functionality of the 74LS107 J-K FF and the 74LS74 D FF. Finally, we will construct a clocked D FF from simple gates.

We have also studied the shift register and counter in class. Shift registers are generally used to convert serial data (i.e., data received on a single line, bit-after-bit) to parallel data (i.e., data that may be transmitted simultaneously on a number of parallel lines, generally referred

to as a bus), or to convert parallel data to serial data. Binary counters usually count the number of pulses from a clock, or astable (“free running”) multivibrator – they are crucially important in computer systems, which almost always employ sequential logic whose events are controlled by clocks and counters. Both are generally composed of bistable circuits with different combinations of inputs and clocking.

- **Serial-to-parallel shift register:** Takes in data serially (bit by bit) and makes it available in parallel, generally to a parallel (multi-wire) data bus. We will study this device today.
- **Parallel-to-serial shift register:** Takes in data from a parallel data buss, and shifts it out serially to a one-wire data buss. Not studied today (but see the work assignment at the end of the lab).
- **Binary counter:** Counts serial pulses on a “clock line.” May be either “ripple” (each stage output clocks the next input) or synchronous (or “parallel” – all stages clocked in parallel).

In order to demonstrate the circuit mechanics of the serial-to-parallel shift register and the simple binary ripple counter, we will build these circuits from “building blocks” of flip-flops. We will use the 74LS74 D FF to build a 4-bit serial-to-parallel shift register, and the 74LS73 J-K FF to construct a 2-bit parallel counter.

4. Experimental Equipment List: The following experimental components are required for this experimental procedure:

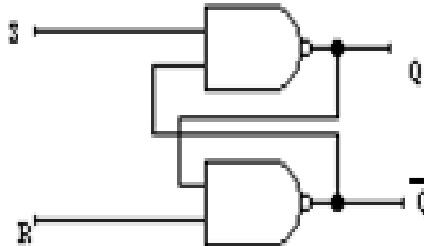
- **IDL-800 Digital Lab. Circuits Evaluator** (“breadboard” unit with test equipment and power supply built in)
- **IDL-800 User Manual** (as required)
- **SN 74LS00 Quad NAND and 74LS04 Hex Inv. Dual In-Line packages (DIPs – digital logic kit)**
- **SN 74LS73 JK FF (1) and 74LS74 D FF (2) (both in digital logic kit)**
- **SN 74LS163 binary counter and 74LS195 serial-to-parallel shift register (digital logic kit)**
- **SN 74LS107 J-K FF DIP (digital logic kit)**
- **Breadboard wire connection kit**
- **Pin assignment diagrams for circuits noted above (see last page)**

5. Pre-Work: Study class notes on bistable circuits. Study the architecture of the R-S, clocked R-S FF’s, the JK FF and the D FF shown in Tokheim. Also study the class notes on the serial-to-parallel shift register and binary counter (synchronous and ripple) circuits.

6. Experimental Procedure:

1) R-S FF:

- Find the 74LS00 chip and plug it into the board as you did the chips last week. Connect pin 7 to ground (0V) and pin 14 to +5V as before. Note that there are 4 equal NAND circuits on the chip; any two may be used in the circuit connection below (refer to the pin-out diagram as needed).



- Connect two of the NAND gates in the 74LS00 as shown above (refer to the 74LS00 pin-outs on the data sheet).
- Connect the two pulse switches to the open NAND gate inputs (those that are not cross-connected to the opposite outputs). Make sure both inputs (switch positions) are 1, since the R-S FF is activated by negative logic (S and R go “low” to set and reset). Connect the NAND gate outputs to LED inputs. Note that either output may be initially designated as Q.
- Turn on the power. Verify the LED condition. The FF may be activated in an arbitrary state, so that you may have either one of the LEDs illuminated. Toggle the S switch (to 0 and back). The Q LED should come on if it was off, and the \bar{Q} LED should be out. Now toggle the R pulse switch. The Q LED should turn off, and the \bar{Q} LED should turn on.
- Note that if neither switch is toggled, the outputs remain in their current state. Now turn both pulse switches on (to 0). The LEDs should both go on. This is a forbidden (unstable) state for the R-S FF, and must be avoided – note that when you release the switches, the resulting state of the FF is not predictable. Set and reset the FF several times to get the “feel” of the circuit.
- Turn off the power and disconnect the circuit connections.

2) D Flip-Flop:

- Plug in the 74LS74 D-type flip-flop and connect ground to pin 7 and 5V to pin 14 as usual. This is a two-circuit dual in-line package (DIP). Referring to the 74LS74 pin-out diagram, choose one of the two D FFs on the chip and connect the input switches to the D and Preset inputs. Since the preset is negative-true logic input, make sure the switch is set to 1. Connect the pulse switches (the negative-true outputs) to the Clock and Clear inputs. The Q and \bar{Q} outputs should be connected to LED inputs.
- Turn on the power. The D FF may power up in either state, so toggle the Clear pulse switch to initialize the circuit. After you do so, the Q LED should be off, and the \bar{Q} LED on. Toggle the Preset switch (to low and back) and notice that the FF “sets” – that is, Q goes to 1 and its LED lights. The Preset switch allows an initial “on” state to be set before any clocked data is introduced into the FF, if the circuit requires an initial “on” condition. Toggle the Clear switch to reset the FF once more.
- Toggle the Clock pulse switch with the D input switch still set at 0. Notice that the FF does not change state. Now set D input to 1 (5V), and re-toggle Clock. Note that the D FF “sets,” that is, as with the Preset input, the Q goes to one (its LED lights) and the \bar{Q} goes to 0 (its LED turns off).
- The D FF can now be reset by setting the D input to 0 once more and re-pulsing Clock. Try these various inputs (Clock with D, Preset, Clear) and observe the circuit operation. Note that simultaneous switching of Clear and Preset results in both Q and \bar{Q} going to 1 (both LEDs will light). This is a forbidden state and will not persist if either Preset or Clear is

released. The reason we say that the state is “forbidden” is that it is unstable and is not a state in which the FF will remain when inputs are taken to their non-active states.

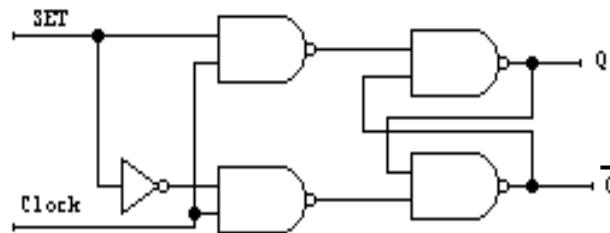
- Turn off the power and disconnect the circuit connections.

3) J-K FF:

- Plug in the 74LS107 J-K-type flip-flop and connect ground to pin 7 and 5V to pin 14 as usual. This is also a two-circuit DIP. Referring to the 74LS107 pin-out diagram, select one of the two J-K FFs and connect the input switches to the J and K inputs. Connect the pulse switches (the negative-true outputs) to the Clock and Clear inputs. The Q and \bar{Q} outputs should be connected to LED inputs.
- Turn on the power. The FF may power up in an undefined state, so toggle the Clear pulse switch to initialize the circuit. After you do so, the Q LED should be off, and the \bar{Q} LED on.
- Both J and K should be set to 0. Now set J to 1 and toggle the Clock pulse switch. Notice that the FF changes state to the “set” state ($Q=1, \bar{Q}=0$). Now set the J input to 0 and the K to 1 (5V), and re-toggle Clock. Note that the FF “resets,” that is, the Q goes to 0 (its LED extinguishes) and the \bar{Q} goes to 1 (its LED turns on).
- Now set the J-K inputs both to 1. Press Clock. Note that the FF “sets” again. Toggle Clock again – the FF now resets. Press Clock several more times noting that with both J and K at 1, the J-K FF simply shifts to the reverse state when Clock is pulsed. Now switch both J and K to 0. When Clock is toggled, there is no change in the outputs. Now try to set various states while holding Clear low. Note that the FF remains “reset” as long as Clear is low, regardless of the state of Clock or J or K. This well-ordered design prevents the “forbidden state” of the R-S FFs – notice that regardless of the input, the J-K FF is in a stable state. Experiment with the J-K FF and get a feel for its operation and for the prevention of a forbidden state.
- Turn off the power and disconnect the circuit connections.

4) Construction of a Clocked D FF:

- A simple clocked D FF may be made with a 74LS00 Quad NAND gate and a 74LS04 Inverter. Note the diagram below.



- Locate the NAND and Inverter chips, and plug in as usual (pin 7=0V, pin 14=5V). Connect the four NAND gates of the 74LS00 as shown (choice of which gate in each position is arbitrary – use the pin-out diagram as required). Connect a switch to one NAND input as shown and also to an inverter input. Connect the output of the inverter to the other forward-positioned NAND. Connect the + output of a pulse switch to the other two inputs on the forward NANDs. The output of the two downstream NANDs should be to two LEDs.
- Turn on the power. Once again, the FF can come up in an arbitrary state, so with the switch for the D signal in the low (0) position, toggle clock. The FF should reset ($Q=0, \bar{Q}=1$ and the Q LED should be off, the \bar{Q} on). Now put the D switch in the on (1) position and toggle clock. The FF should set (Q LED on, \bar{Q} LED off).
- Note that although our FF construction is very simple (no independent Set and Reset – all functions must be clocked), there is no possibility of a forbidden state. The Set/Reset inversion pair assures that either the FF Set or Reset is always high, so that the inputs always result in a stable situation.
- Take some time to exercise the FF and get used to its operation. Then turn off the power and dismantle the circuit.

5) **4-Bit Serial-to-Parallel Shift Register:**

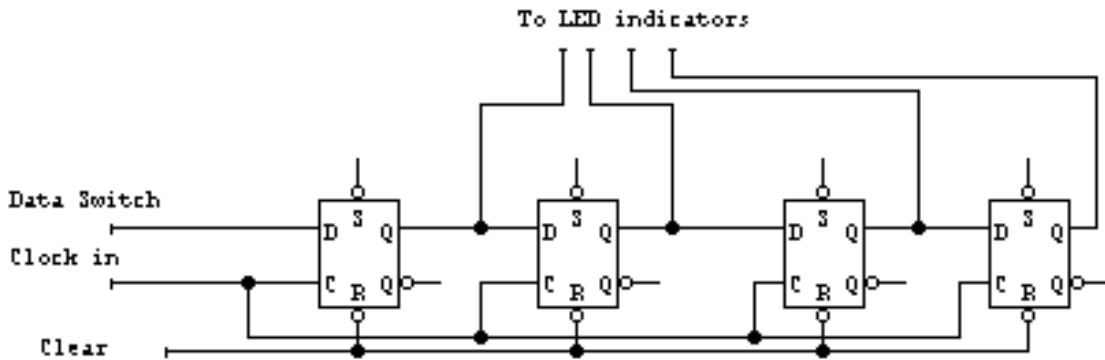
- Locate the 74LS195 serial-to-parallel shift register and plug it into the prototype board. Note: for all the following instructions on connections of circuits in parts 1)-4), please refer to the appropriate chip diagram on the last page of these instructions. Connect pins 8 and 16 to ground and +5V, respectively. Connect the parallel output pins Q_A - Q_D to LED indicators. Connect the serial-in input pins J and K (pins 2 & 3) to one of the data switches, making sure that the switch is set to 0, and the clock input to the clock generator output. Connect the clear input to one of the negative-true pulse-switch outputs.
- Turn on the power. Press clear and make sure that all 4 LED's are dark. Set the clock frequency to 1 Hz and the clock amplitude to about $\frac{1}{2}$ max. (indicator on the clock level knob pointing about straight up). The shift register should be operational at this point, but since the data switch is set to 0, all LED's will remain dark. Set the switch to 1. You should immediately see serial bits passing from the lowest stage (A) to the highest (D) each time the clock pulses. After four clock cycles the output data bits should all be 1. Return the data switch to 0 and the shift register will be filled serially with 0's again. A little rapid switching of the data switch at this point can alternate 1 and 0 bits being shifted into the register. If you wish, attach the data input to a pulse switch and you can control alternate 1's and 0's more easily.
- Repeat this procedure until you are familiar with the shift register operation.
- Turn off the power and disconnect the circuit.

6) **Binary Counter:**

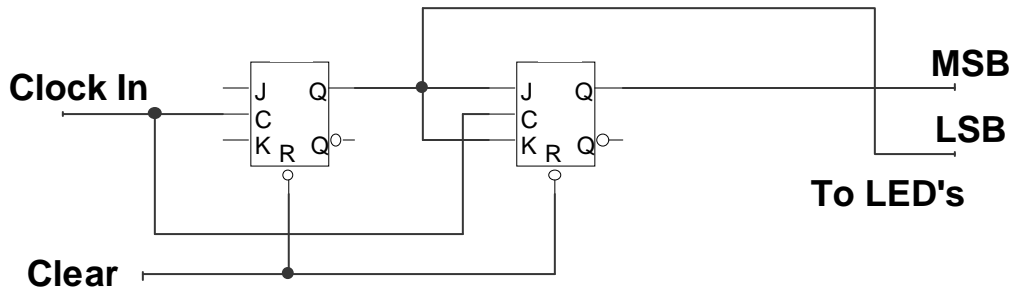
- Plug in the 74LS163 binary counter and connect +5V and ground as before. Connect clock input to the clock pulse output (still set to 1 Hz), and clear to the true-negative pulse switch output. Since we are ignoring the data-inputs capabilities of the '163, do not connect data pins. Connect the LED inputs to Q_A - Q_D counter outputs (Q_A is least significant bit or LSB). Turn on the power and set up the clock amplitude to about $\frac{1}{2}$ max. Clear the clock and watch the LED outputs. The counter should count the clock pulses sequentially, from 1 to 15, and then reset to 0 automatically on the 16th pulse. Make sure that this occurs. Note that clearing the clock during the middle of a cycle merely starts the counter at 0 again and counting resumes. Note that the counter does a "synchronous clear," meaning that if clear is pulsed, the actual clear occurs on the next clock pulse. For purposes of our exercise, that makes no difference in the counting sequences of interest.
- Repeat the counting sequences until you are familiar with the counter operation.
- Turn off the power and disconnect the circuit connections.

7) **Building a Serial-to-Parallel Shift Register Using 74LS74 Dual D FF's:**

- As noted above, a serial-to-parallel shift register is a connection of a group of bistable circuits which can receive information serially and make it available in parallel. In this section of the laboratory procedure, we will construct a 4-bit serial-to-parallel shift register from 74LS74 D FF's.
- Insert two 74LS74 FF's into the prototype board and connect power and ground. Connect all 4 clear inputs (one clear line on each of the 4 FF's on the two chips) to a true-negative pulse switch. The Q output of each FF should be connected to the D input of the next FF as shown on the next page:



- Connect the clock inputs as shown with the clock frequency still set to 1 Hz as before. The first D input should be connected to a positive-true pulse switch (normally in 0 position). Make sure that all Q outputs go to LED inputs; the Q with the data switch input is the LSB.
 - Turn on power and set clock amplitude as before. The FF's should be operating as a serial-in shift register, but all should be unlit, since they are shifting in 0's (the data switch is set to 0). Now set the pulse data switch to one. A series of 1's should shift into the four FF's just as they did into the 74LS195, at the 1-Hz clock rate. As before with the '195, you should be able to rapidly push the data switch and get alternating 1's and 0's to shift through the shift register.
 - Operate your "home-grown" shift register until you have a good feel for circuit operation.
 - Turn off the power and disconnect the circuit connections.
- 8) Building a Parallel or Synchronous Binary Counter from a 74LS73 Dual J-K FF:
- One problem with "modern" so-called TTL or bipolar circuitry (which is the name for the circuits in the chips we are using) is that fewer flip-flops are being made as master-slave. Our 74LS73 is an "edge-triggered" FF, which was not covered in class.
 - Although this FF should operate "just like" a master-slave FF, it is very sensitive to timing and input signal level, which makes construction of a counter with edge-triggered FFs more difficult. For this reason, we will construct only a two-bit synchronous or parallel counter.
 - Plug a 74LS73 JK FF into your prototype board. **NOTE: BE VERY CAREFUL TO CHECK THE POWER INPUT PIN CONFIGURATION AND CONNECT THE 74LS73 CAREFULLY! THE 74LS73 POWER INPUT PINS ARE LOCATED VERY DIFFERENTLY FROM THOSE WE HAVE BEEN USING.**
 - Connect the two FFs in the 74LS73 as shown below:



- Note that leaving the LSB J and K open on the left ff is equivalent to a '1' on those inputs, so we have made both the ffs into Toggle FFs. You can also connect those J and K inputs to +5 V, if you wish.

- In counting, the first counter stage is toggled by every clock pulse; the second stage is clocked or toggled when the output of the first stage is a '1'. This is a so-called parallel counter such as we studied in class.
- Turn on power and set clock as before. Clear the counter (the "Clear" should be connected to a momentary-low pulse switch). Note that the counter immediately begins to count. It should count up to 3 and immediately reset to 0 on the next clock pulse. It will continue to count regularly until the power is turned off.
- Operate your "home-grown" counter sufficiently to become familiar with its operation.
- As noted above, the 74LS73A, the "edge-triggered" circuit that you are using, is notoriously sensitive to signal and voltage levels. You may have to "experiment" with the clock signal level (turning the level higher or lower) to get the counter to count properly.
- Turn off the power and disconnect the circuit connections.

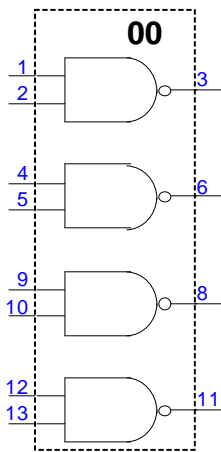
7. Equipment Disassembly: The experimental procedure is complete. Please disassemble the circuit wiring, replace in the wiring kit box and replace it as you found it in the cabinet. Turn in the logic circuit kit to the instructor or the TA. Make sure that your work area is clean.

8. Laboratory Report: As usual, your laboratory report should follow the form given. In your write-up, discuss the operation of the circuits and the verification of the function of each.

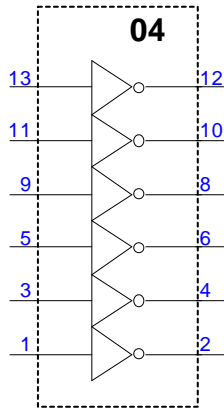
Also include the following items:

- Discuss your experience in the laboratory and any problems with the procedure.
- Show the circuit hook-up for the R-S FF and clocked D FF circuits that you made up in parts 1 and 4 of Section 6. Include these in your report. Make sure to include the pin numbers of each gate used.
- Include the truth tables for the two FFs that you constructed. Also make up the truth table for the 74LS107 in your report.
- For the D FF shift register that you constructed, make a wiring diagram similar to the one in the instructions, but including all pin numbers in the wiring and showing the package outlines so that the wiring of the chips is clearly delineated.
- For the JK FF binary ripple counter that you built, draw a similar diagram, showing the package outlines and all pin connections.
- Now consider a 4-bit parallel-in, serial-out shift register. Using D FF's, design the register and show a timing diagram of the loading and shifting out of data. Assume that the FF's are master-slave, in order to assure separation of stages. Assume that each D FF has a separate "Preset" input, so that each bit may be initially set in parallel, before the serial shifting is begun.
- Discuss any insights gained from the exercises.

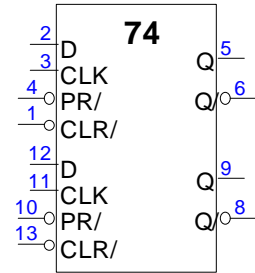
Digital Logic Chip Pin-Out Diagrams



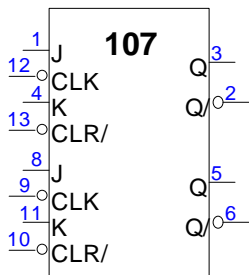
**SN 74LS00 Quad
2-input NAND gate**



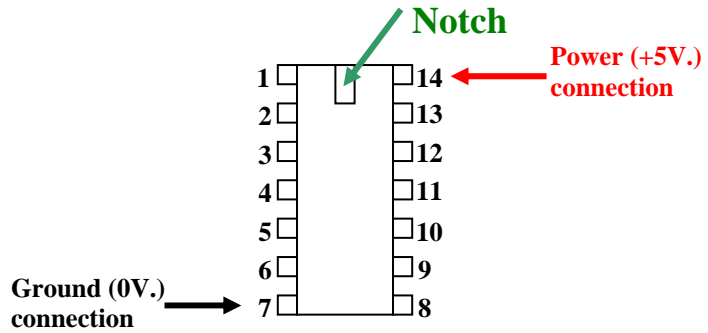
**SN 74LS04 Hex
Inverter gate**



SN 74LS74 Dual D FF



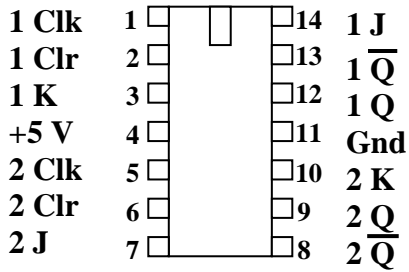
**SN 74LS107 Dual
JK FF**



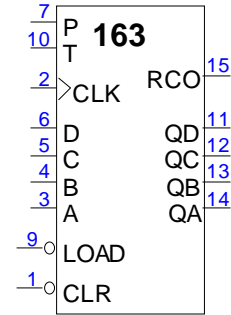
74 LS XXX Chip Outline

Pin-Out Diagrams continued on the next page...

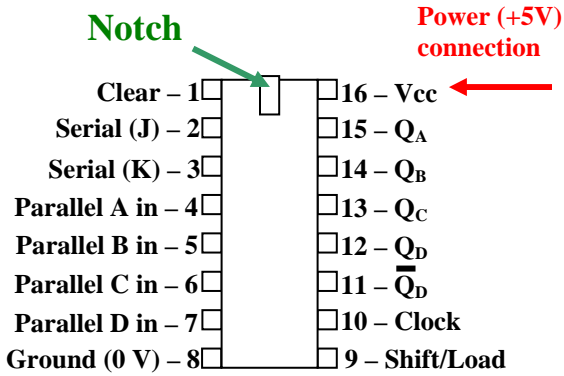
Digital Logic Chip Pin-Out Diagrams



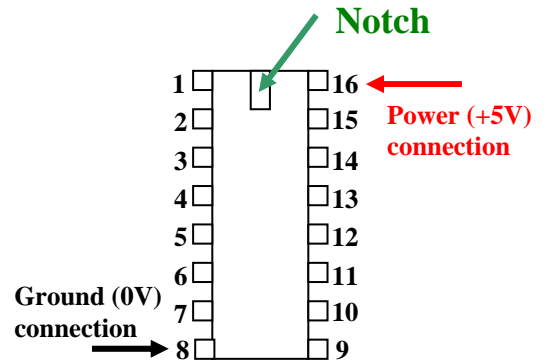
SN 74LS73 Dual JK FF



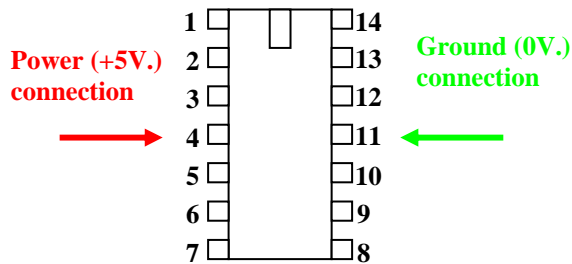
SN 74LS163 Binary Counter



SN 74LS195 Shift Register



Package Outline for 74LS163



Package Outline for 74LS73 – Note unique power connection!!!!!!!
Pin 4 = +5VDC,
Pin 11 = Ground