Simple RS-Flip-Flops can be made from any two 2-input combinational logic gates plus some inverters. Design the following RS flip-flops, labeling S, R, Q, Q-Not (and clock, as necessary). Make sure you label the polarity of R and S when active (+ =1 or – =0).

1. (CLO 4—Seq. Logic) An AND gate, an OR gate, and inverters as needed. Inputs S and R are active low (0).

2. (CLO 4—Seq. Logic) An AND gate, an OR gate, and inverters as needed. Inputs S and R are active high (1).

3. (CLO 4—Seq. Logic) A NOR and a NAND plus inverters as needed. Inputs must be active low (0).

4. (CLO 4—Seq. Logic) A NOR and a NAND plus inverters as needed. Inputs must be active high (1).
5. (CLO 4—Seq. Logic) Construct a clocked RS flip-flop using two OR gates, two AND gates, and inverters. Note that Set and Reset are active in the high (1) state.

6. (CLO 4—Seq. Logic) Given the clocked RS flip-flop shown, plot the output Q versus clock, Set, and Reset as shown below. Remember that Set and Reset are active high (1).