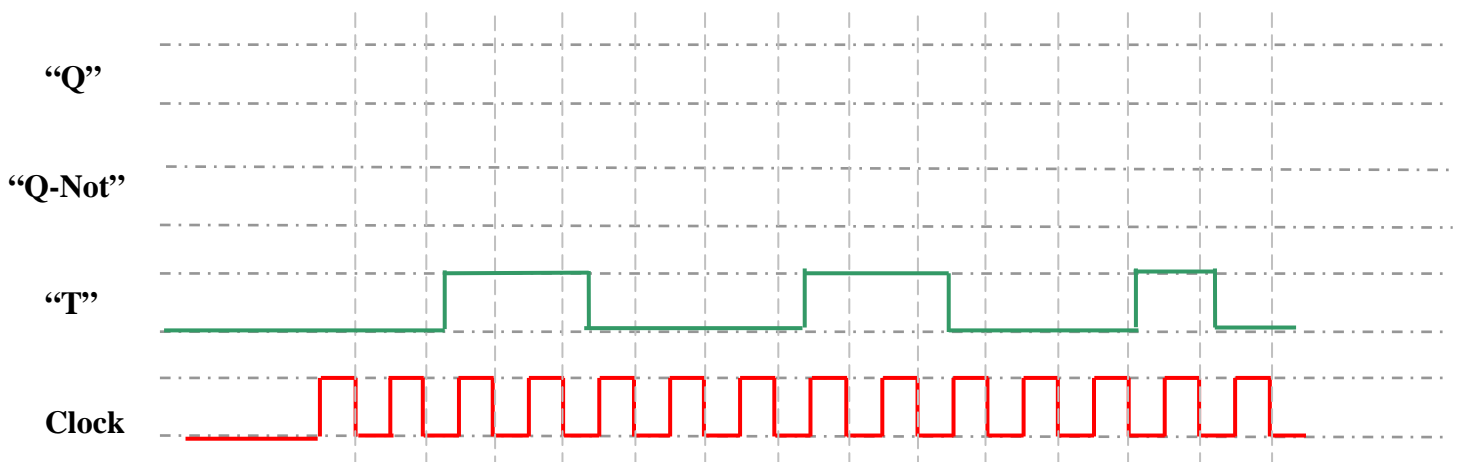


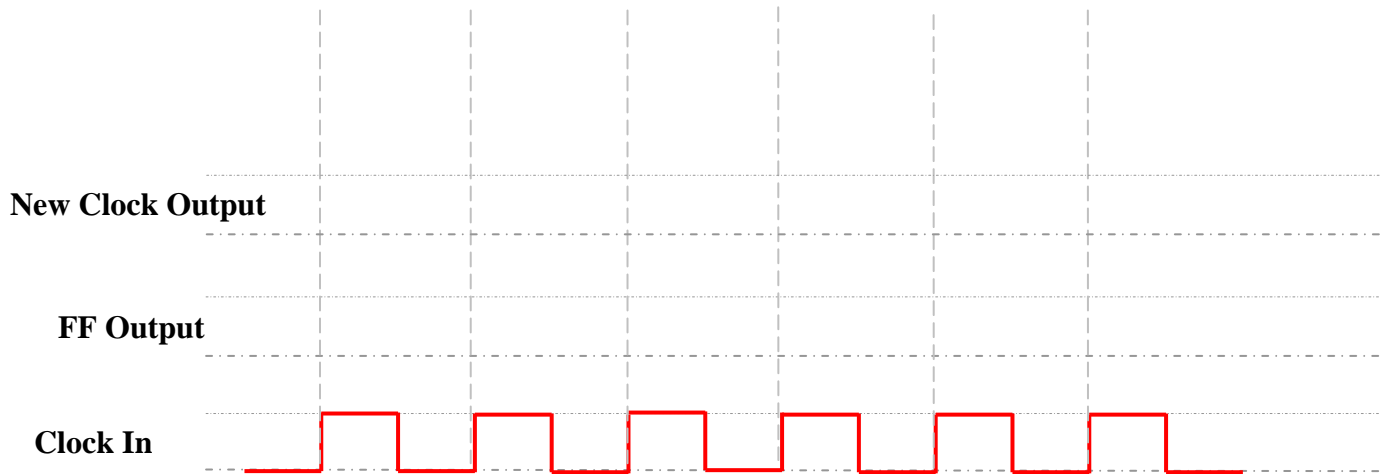
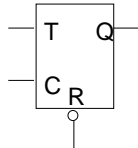
EE 2310 Homework #5 – Clocks and Flip Flops

Name: _____ Student Number: _____

1. Using the design for a T FF shown in Lecture 7, design a simple T Master-Slave Flip-Flop or “counter flip-flop” below, then show the timing diagram for the Q output given the “T” that is shown and the 50-50 clock inputs. “Simple Master-Slave T Flip-Flop” means that you can dispense with most of the input logic that was in the diagram of the T FF in Lecture 7, and still have a usable flip-flop with T and clock inputs.

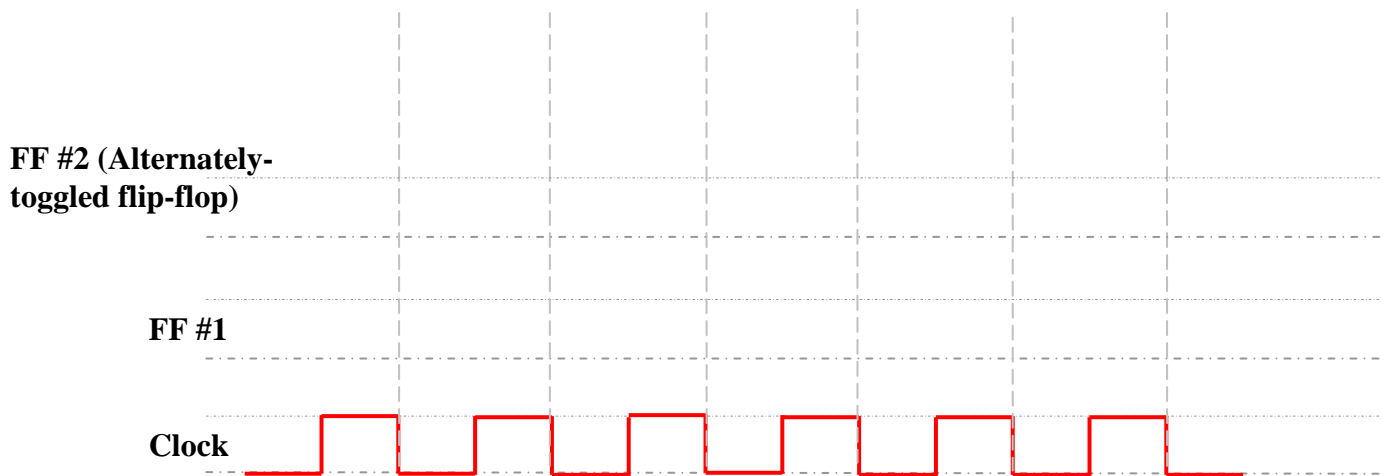
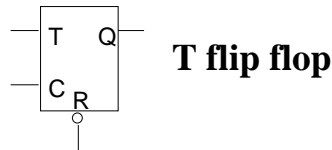


2. Using the T FF shown below, devise a circuit that takes a 50-50 clock input and changes it into a clock output at $\frac{1}{2}$ the frequency that is a 25%-75% clock (i.e., it is logic 1 for one quarter of the clock cycle and 0 for three quarters of the cycle). Also, show the timing below. Note 1: leave the R (reset) line on the T FF unconnected. Note 2: All T FF's are master-slave.



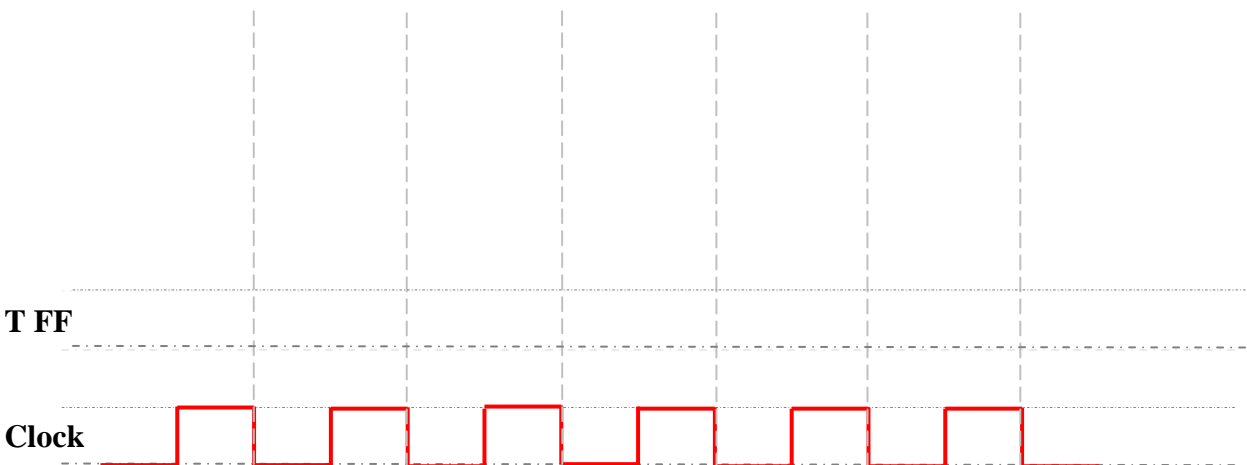
Timing of New Clock at $\frac{1}{2} f$ and with 25-75 Duty Cycle

3. A master-slave toggle flip-flop is to be toggled by every other pulse from an input 50-50 clock. That is, every 2nd clock pulse, it is set, and after another 2 clock pulses, it is reset. Using a second master-slave toggle ff, construct a circuit to assure that the original ff is only toggled as desired. On the timing diagram below, show the timing of the Q outputs for both flip-flops to demonstrate their setting and resetting. Also, use the symbol shown for the T FF. Hints: (1) A T FF must have the T input held high (i.e., to 1) for it to toggle. (2) If you want a T FF to continuously toggle, tie the T input to a “1” permanently (where it is understood that a “1” is really a voltage like 5 V.). (3) Think about the timing of the Q output of the first T FF. Remember, the T FF output changes on the backside (down-going edge) of the clock since it is a master-slave ff. Assume the ff’s run continuously, so there is no need for a reset pulse (leave reset unconnected on both ff’s).



Timing of “Alternate Toggle FF”

4. The T FF shown in the lecture was relatively complicated, in that the inputs included both “T” and “clock.” If T=1, the ff “toggles” on every clock pulse. If T=0, the ff does not toggle at all. We have simplified that flip-flop in problem 1, above – the result still had a T-input, but some of the gates at the FF input were eliminated. Now suppose we want to make a very, very simple T FF that has (1) only one input, the clock, and (2) that always toggles on every clock cycle, to act as a simple “÷2” frequency divider. This allows us to make an even simpler T FF than the one you designed in Problem 1. It will still be a master-slave clocked ff, with much of the circuitry at the inputs eliminated, but even the T-input will not exist. Show the design for that simple “always toggle” T FF below, and the timing diagram for the “Q” output of the ff with respect to the clock input. Hint: You can start with your design from problem 1, and think how to simplify it to get the desired flip-flop.



Timing of “Always Toggle FF