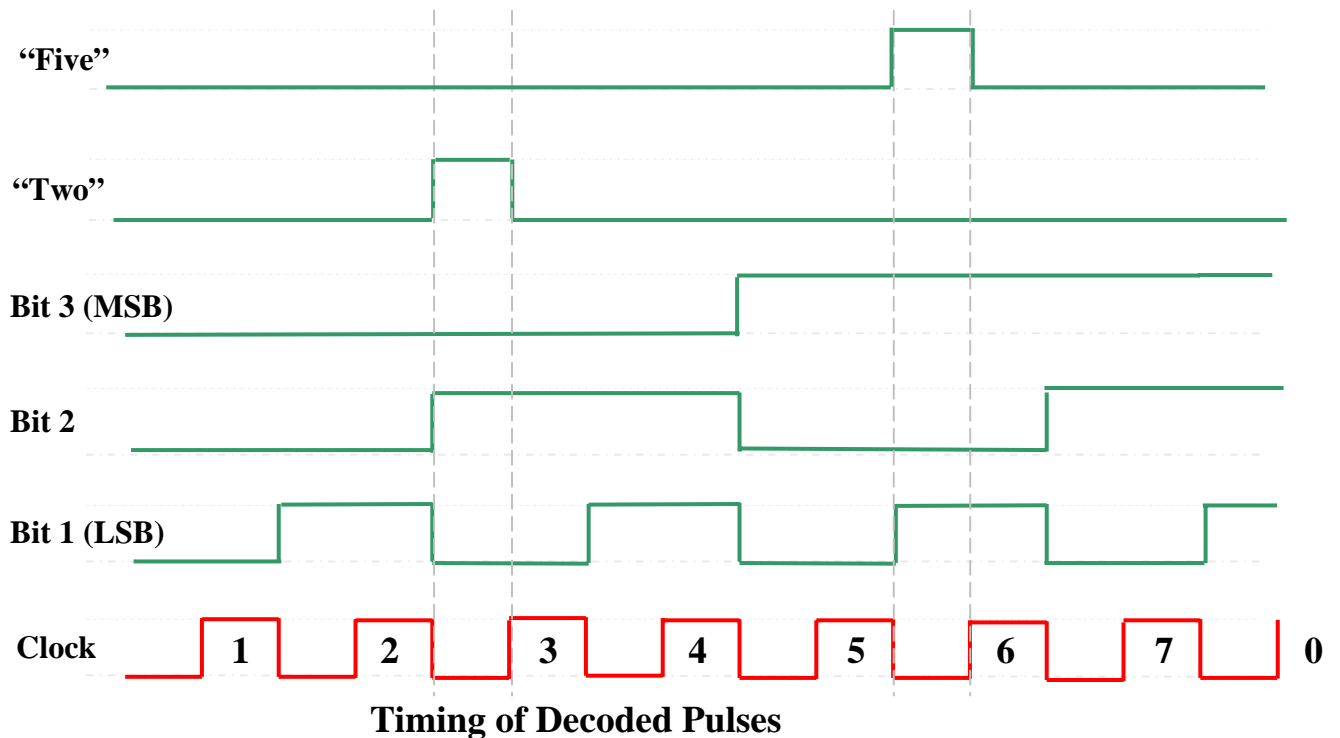
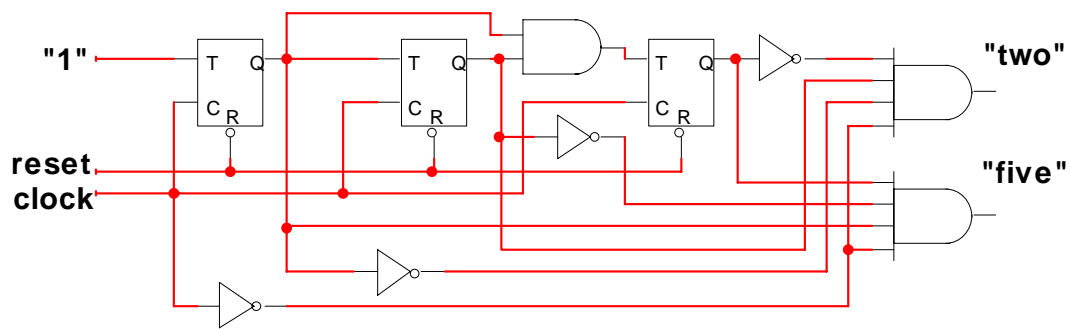
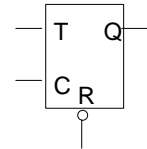


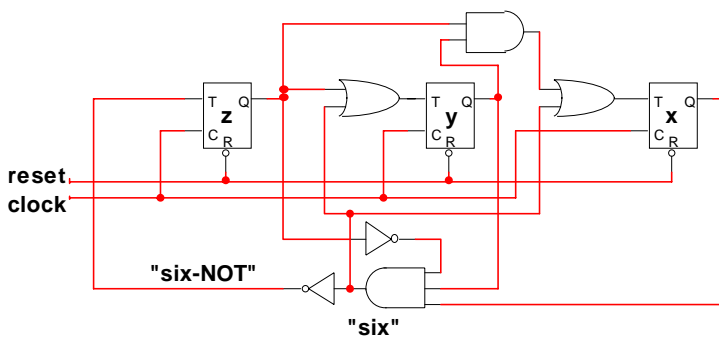
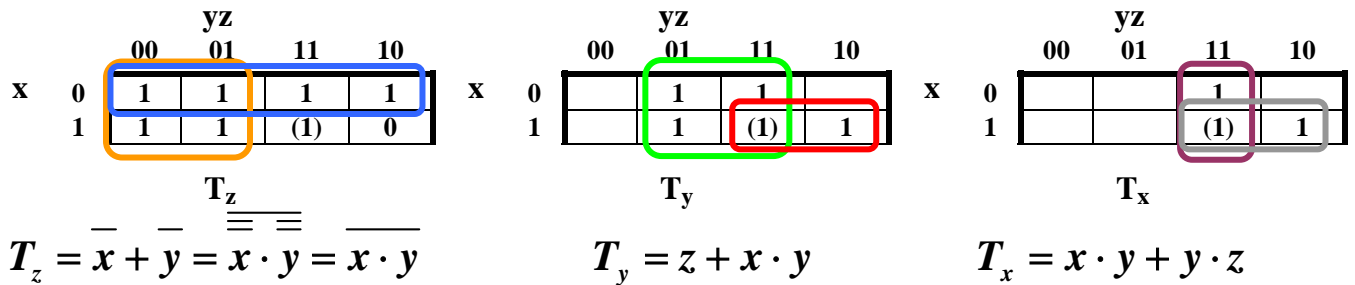
EE 2310 Homework #6 Solutions – Sequential Logic

1. A three-bit synchronous (parallel) counter is to be constructed, and two events decoded from its output. The binary numbers 2 and 5 are to be decoded, ANDed with the inverted clock pulse, and transmitted to another circuit. Thus signals “2” and “5” last $\frac{1}{2}$ clock cycle, after the counter outputs are true; i.e., they are true when clock is false or low. The counter is free-running, and is only cleared at start-up by a common reset pulse tied to all the ff reset inputs. In summary:

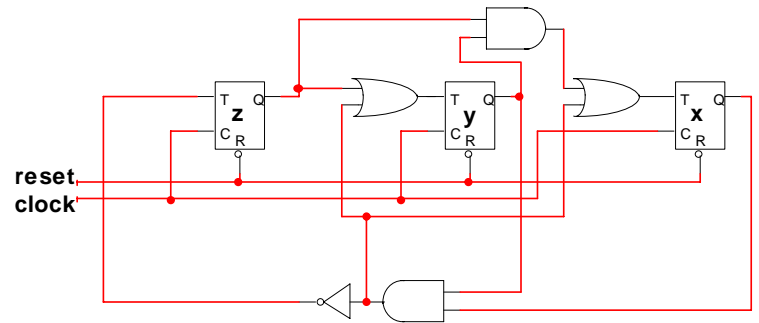
- Counter inputs are clock and reset
- Counter outputs are signals “2” and “5”
- Input signals come from the left, output signals exit to the right
- Use the T ff shown to the right, and show the timing diagram on the form below.



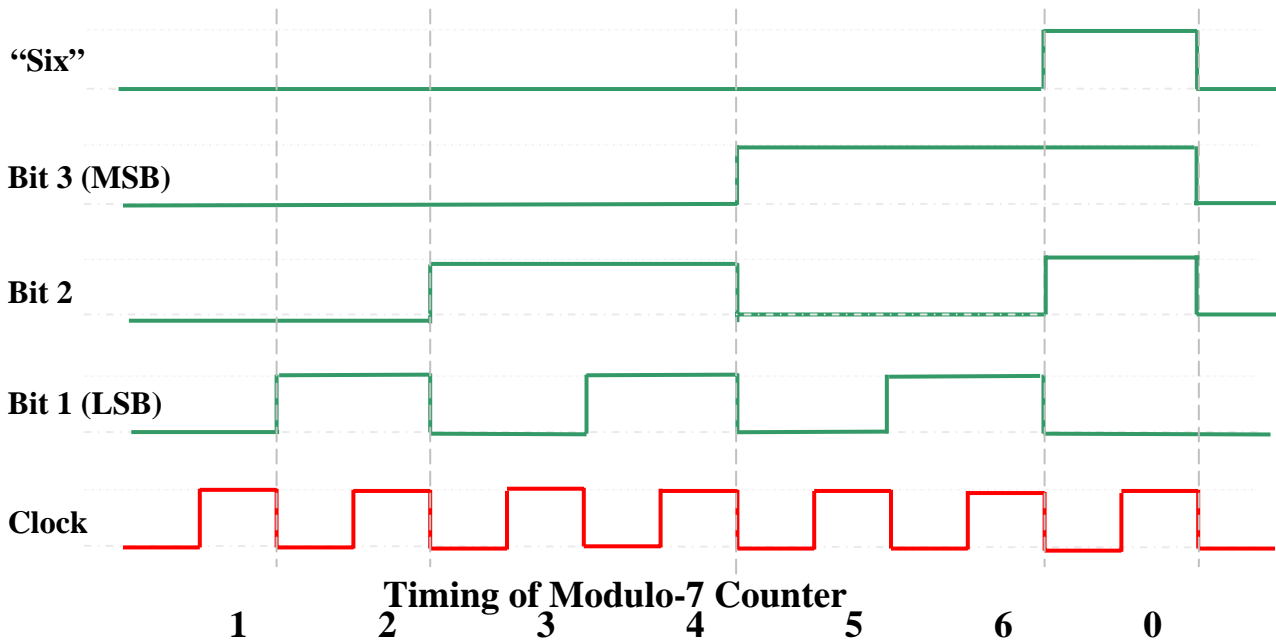
2. Construct a modulo-7 parallel (synchronous) counter from the three T master-slave FF's shown below. That is, the counter should count up to six, and reset to zero on the seventh pulse. Call the stages of the counter x, y, and z. The T-inputs of the stages are then Tx, Ty, and Tz. Remember that for each ff to toggle when the clock input cycles, the T input must be set to logical "1." Construct a timing diagram for clock and the three "Q" outputs of the counter on the chart below. Use either the Karnaugh map method or the "short-cut" method to design the counter. Since the counter flip-flops are master-slave, all outputs change on the down-going or "backside" edge of the clock.



Short-Cut Method (Decoding "n-1")

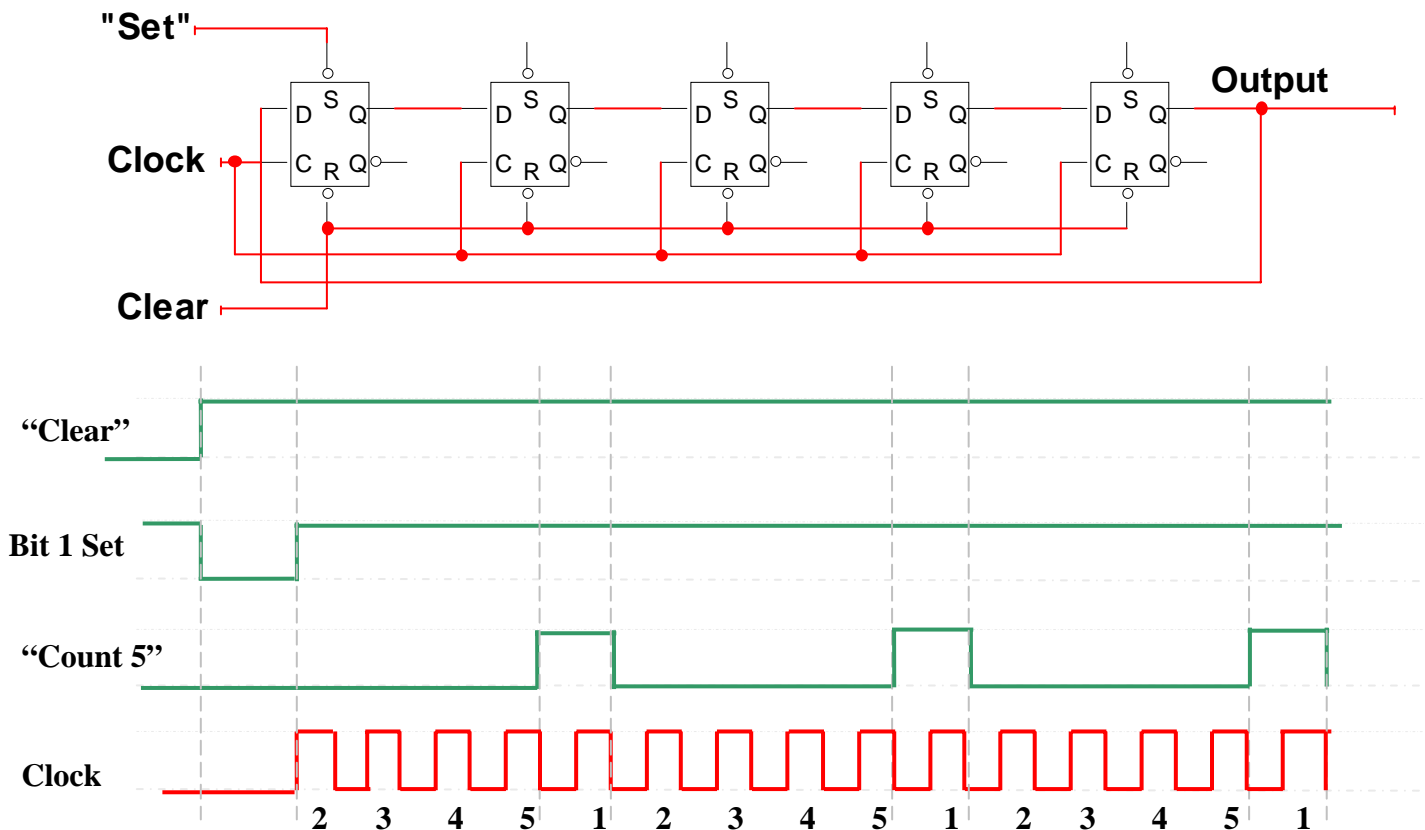


K-Map Method (K-maps shown above)



3. A “ring” counter is a shift register with one bit set to one and the rest set to 0. The last-stage output of the shift register is connected to the first stage, so that the “1” is passed from one stage, or flip-flop, of the shift register to the next, returning to the first stage the next clock cycle after it reaches the last stage. In this way, it “circulates” through all the stages of the shift register in sequence, in what can be regarded as a “ring” or circle of flip-flops whose every output is connected to the next input. If one stage of an n-bit (or n-ff) shift register is arbitrarily selected as the “output,” this output stage will output only 0’s for (n-1) cycles, but a 1 every nth cycle. Thus it functions as a counter which counts n clock cycles by outputting a 1-pulse on the nth clock.

From the five master-slave D-FFs below, construct a 5-cycle “ring” counter. Assume that the ff on the far right is the “output” ff. The timing is shown below for an original “Clear” pulse that clears the counter on startup, and the “set” pulse that originally puts the single “1” in the first shifter stage. After those two pulses, the counter runs continually. Show the rest of the timing of the output “count 5” pulses for the number of clock cycles indicated below. Note: make sure you connect “Clear” to all the counter stage resets and “Set” to the first bit set input. (Note: Start your clock with pulse “2” because the “1” is already in the first ff of the shift register.)



4. In the space below, draw a multiplexer which has only two inputs but four address lines from a 4-bit binary counter. Complete the circuit, which is mainly combinational logic, so that the input “a” is output on count 0 and the input “b” on count 11. Assume the counter runs continuously and the four counter inputs (labeled w-z, w the MSB) are always valid. Each MUX output should last the full count of its respective number. Show the timing on the diagram below. Assume the counter uses master-slave T ff’s.

