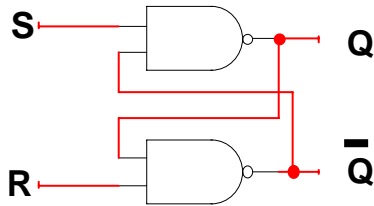
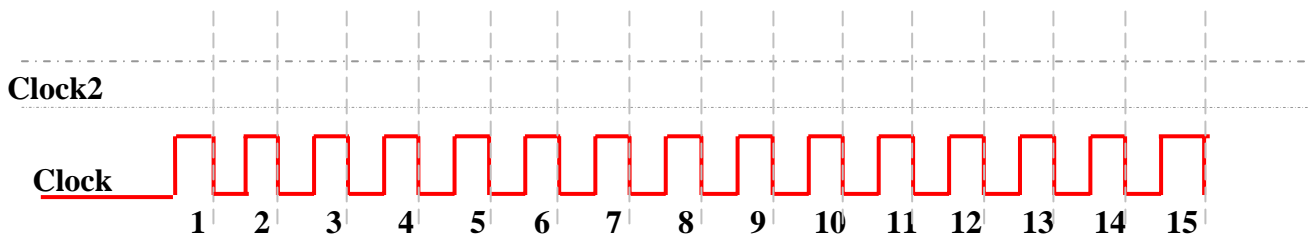
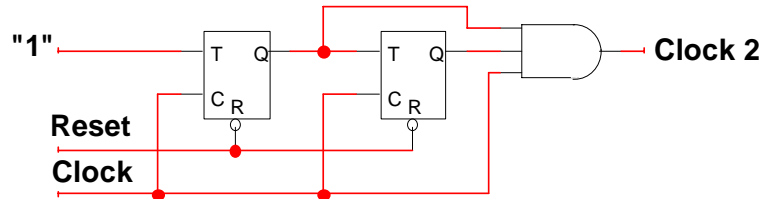


## EE 2310 Worksheet #3B – Flip-Flops and Timing

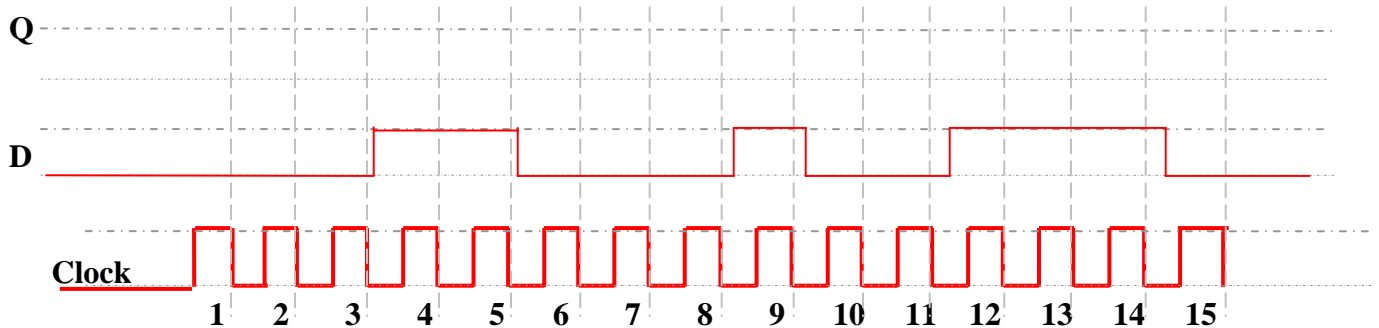
- Suppose we want to have the simple RS flip-flop below be set and reset by positive-going pulses, not low-going ones. How could we achieve that?



- Assume Reset is done before the clock starts below and plot Clock2. The T FF's are master-slave.



- On the timing diagram below, show the timing for the output Q of a simple D flip-flop (non-master-slave) with input D and clock as shown.



- The circuit below is a D Flip-Flop. Label Q, Q-Not, D, and Clock appropriately. What is the mysterious input "X"? Label it appropriately also.

