

# Introduction for CDC Lab and Collaborations with Industry

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## Hardware/Software Co-design Lab. for DSP and Communications (CDC lab.)

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- The largest amount of existing computer systems are systems consisting of both hardware and software components.
- Advances in process technology and ever increasing demand of smarter, cheaper, power-conscious systems have fueled the needs for better tools to implement such systems.
- The real need around the high-tech industry.
- We now have the leading researchers in this area at UTD.
- More information can be found in <http://www.utdallas.edu/~edsha>

## Codesign Lab. for DSP and Communications (CDC)

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- Play an important role with Embedded software center in CS and DSP group in EE.
- DSP group in EE focus on DSP algorithms such as source coding, channel coding, compressions, etc.
- Embedded software center focus on software engineering issues such as specification, testing, verifications, component based design-flow methodology, etc.
- **CDC Lab.** focus on **design and implementation issues** such as embedded architectures, network architectures, wireless communication components design, multi-processor systems, hardware component designs, real-time systems, design space explorations, code generations, HW/SW interface, memory issues, etc.

## Goals of the CDC Lab.

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- Develop strong research program in hardware/software co-design for DSP and communications.
- Improve education through research projects and courses that give hands-on experience on implementing DSP and communications applications.
- Promote collaboration between the members, other groups on campus, in other universities and in industry.
- Through collaboration and training with industry, **provide industry with expertise, broad knowledge, and highly skilled engineers for possible future employees.**

## Research Areas in CDC Lab.

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- **Applications:** real-time controllers, DSP, routers, switches, wireless communications, virtual conferencing, etc.
- **ASIC designs of DSP and Communication components:** 3G wireless components such as wireless modem, equalizer, channel estimator, channel codec, source codec, etc.
- **Design space exploration and performance evaluations:** How many processors (DSP or general processors) and which types? How much on-chip memory, off-chip memory? How is the bus? What kinds of hardware components, etc. Consider timing, power, area and cost?
- **Software for co-design:** real-time operating systems, process scheduling, software synthesis, system integration, retargetable compilation.

## Research Areas in CDC Lab., cont

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- **Optimal code generations:** the most time and power efficient codes. It is hard for multiple processors or VLIW processors.
- **Computer and network architectures:** hardware/software interfaces, distributed and multiprocessor architectures, fault tolerant and re-configurable platforms.
- **ASIC designs for DSP and Communication cores:** low power, and time efficient components such as MAC units, FFT, DCT, Viterbi and turbo channel codec, adders and multipliers.
- **Hardware/Software Codesign of network components:** Design of special-purpose parallel architectures for implementing functions required in high performance networks to ensure quality of services.

## Research Areas in CDC Lab., cont.

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- **Resource Optimization in Circuit Switched Wavelength Division Multiplexing (WDM) Optical Networks.**
- **Core Router Design for Burst Switched WDM Networks:** Design and implementation of important components for operations such as burst routing, burst forwarding, data channel scheduling and control channel scheduling in a core router of WDM networks.
- **Edge Router Design for Burst Switched WDM Networks:** Design and implementation of important components for operations such as burstification of packets, burst routing and switching, channel scheduling in an edge router of WDM networks.
- **Architecture of Packet Switching All-Optical WDM/TDM Networks:**  
Design of new architectures of future all-optical packet switching networks that use both WDM and TDM techniques.

## Equipment and Personnel of CDC Lab

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- Faculty: Dr. Edwin Sha, Dr. Yuke Wang and Dr. S. Q. Zheng
- Students: Currently 4 Ph.D. students, another Ph.D. student will arrive UTD in Spring 2001 and several more grad. students including Master degree students are being recruited.
- Equipment: Under development. 12 computers with DSP software and boards such as TI Code Composer Studio, TI TMS 320C6201/6701 Evaluation modules and TI TMS 320C54X Evaluation modules. FPGA boards.

## Grants with Industry

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- Mutual Benefits. Most cost effective ways. Get several faculty members who have broad knowledge and know the state-of-art technology and research students working on designated projects.
- Start with short-term and then build up long-term projects.
- Goal: spend the minimum amount of cost and time and get the most done.
- Budget: about \$100K a year. It can be flexible. Lets just list 2 possible budgets in the following.
- Have at least 2 graduate research assistants and faculty members working together.

## Possible Budget 1. It is flexible.

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- Total budget: about \$110K a year.
- University Ordinary Grant: \$56000 + 48% indirect cost = \$82800  
Includes 2 RA one-year salaries, tuitions, fringe benefits (23%), materials and supplies.
- Consulting fees with faculty: \$30K.
- Please come to talk with any faculty members in CDC lab. for more information.

## Possible Budget 2. It is flexible.

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- Total budget: about \$86K a year.
- University gift grant (no indirect cost): \$56000. Includes 2 RA one-year salaries, tuitions, fringe benefits (23 %), materials and supplies.
- Consulting fees with faculty: 30K.
- Please come to talk with any faculty members in CDC lab. for more information.

## Dr. Edwin Sha (Introduction)

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- Ph.D. from *Princeton University*. Worked in U. of Notre Dame for many years before came to UTD in 2000. He is currently a full professor in CS at UTD.
- **Research Interests:** Hardware/Software Co-designs for Communications and DSP, Real-time Systems, DSP Architecture, Fault Tolerance, Parallel Architectures and systems, Operating Systems, Low Power Systems, High-Level Synthesis in VLSI, CAD for Application-specific Systems, Loop Scheduling for DSP, Java Systems, Software Tools for Parallel and Distributed Systems
- Editor for **IEEE Transactions on Signal Processing**. (Responsible for the areas of system implementations, architectures and programming systems.)
- Editor for **Journal of VLSI Signal Processing**.

## Introduction, cont.

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- Grants with **NSF, DARPA, AT&T, Cadence, etc.**
- **NSF Career Award** and Notre Dame Teaching Award.
- Program committee in numerous international conferences.
- Program Chair for IEEE Great Lakes Symposium on VLSI. Program Co-Chair for International Conference on Parallel and Distributed Computing Systems (PDCS 2000) in Las Vegas, 2000.
- Program Chair for International Conference on Parallel and Distributed Computing Systems (PDCS 2001) in **Dallas**, Texas, August 2001.
- Published more than 130 papers in referred conferences and journals.

## Dr. Edwin Sha's Research Areas

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- **Automatic Parallelization:** Develop new techniques to fully parallelize DSP applications; consider synchronous data flow graphs and develop retiming technique for SDFG.
- **Real-time and Low-power Systems for DSP and Communications:**  
Produce the most time efficient schedule and architecture with multiple processors or VLIW systems. Develop low power scheduling, Hardware/software codesigns.
- **Memory Issues for DSP and Communication Applications:** What is the best size for on-chip memory. Develop data access hiding techniques: partitioning, prefetching and loop scheduling which produce a completely balanced schedule.

## Dr. Edwin Sha's Research Areas, cont.

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- **Real-time and Fault Tolerant Embedded Systems Designs:** Design and implement hardware components and software systems which guarantee real-time and fault tolerant properties.
- **The Design of Parallel Java Stack Machines.**
- **Design Space Explorations:** Obtaining a set of acceptable designs containing which types and how many functional units.
- **Optimal Memory Hierarchy Placement and Replacement:** The traditional MIN algorithm is not optimal if we can place data in any given level of memory system. We have designed a truly optimal algorithm.
- **Quality of Service Analysis and Design Issues for Networking**
- Please check <http://www.utdallas.edu/~edsha>

## Dr. Yuke Wang (Introduction)

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- Dr. Yuke Wang has many years of experience in designing VLSI, DSP algorithms, CAD, etc. During 1996-2000, Dr. Wang has co-authored papers with more than 12 IEEE/ACM Transactions journal papers.
- He has obtained important and fundamental results in several areas of CAD and circuit design. In particular, he improved the algorithm for **Chinese Remainder Theorem**, which was originally discovered by Gauss in 1801 and is widely useful in DSP, error correction, and security.
- He has designed **adders** which are better than almost all previous adders in terms of power and timing including the carry-look-ahead adder, carry-select adder, conditional sum adder, prefix adders, and signed-digit based adders.
- For more information, please check <http://www.utdallas.edu/~yuke>

## Dr. Yuke Wang's Research Areas

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- **ASIC Design of DSP and Communication Cores:** MAC units in DSP processor, FFT, DCT, Viterbi and Turbo channel codec, arithmetic circuits such as adders and multipliers.
- **Computer Aided Design for DSP and Communication Circuits:** high-level synthesis and logic synthesis.
- **Implement Communication Systems Using DSP Processors:** OFDM systems, 3G wireless systems-wideband CDMA, UWC-136, EDGE, CDMA 2000; Wireless LAN - Bluetooth, SWAP, IEEE802.11; Power line communication modem.
- **DSP Processor Performance Evaluation:** superscalar, SIMD, VLIW processors.

## Dr. S. Q. Zheng (Introduction)

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- Dr. S. Q. Zheng received Ph.D. from Univ. of California at Santa Barbara. He is currently a full professor in CS department at UTD.
- He has published more than **150** research articles and written a well-known book on **parallel computing using optical interconnections**.
- He has many years of experience in computer architecture design, VLSI, Hardware/software codesign, optical interconnect and telecommunication and networks.
- He has been served as editors for 5 journals and program chairs for more than 5 international conferences.

## Dr. S. Q. Zheng's Research Areas

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- **Resource Optimization in Circuit Switched Wavelength Division Multiplexing (WDM) Optical Networks:**  
Design and analysis of wavelength assignment algorithms, and converter and amplifier placement algorithms.
- **Core Router Design for Burst Switched WDM Networks:**  
Design and implementation of important components for operations such as burst routing, burst forwarding, data channel scheduling and control channel scheduling in a core router of WDM networks.
- **Edge Router Design for Burst Switched WDM Networks:**  
Design and implementation of important components for operations such as burstification of packets, burst routing and switching, channel scheduling in an edge router of WDM networks.

## Dr. S. Q. Zheng's Research Areas (cont.)

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- **Architecture of Packet Switching All-Optical WDM/TDM Networks:**  
Design of new architectures of future all-optical packet switching networks that use both WDM and TDM techniques.
- **Hardware/Software Codesign of Network Components:**  
Design of special-purpose parallel architectures for implementing functions required in high performance networks to ensure quality of services.
- **Interconnection Networks for Telecommunications:**  
Design of special interconnection networks for switching matrices used in telecommunication switches and data network routers.