

A Novel Multiplexer-Based Low-Power Full Adder

Yingtao Jiang, Abdulkarim Al-Sheraidah, Yuke Wang, Edwin Sha, and Jin-Gyun Chung

Abstract—The 1-bit full adder circuit is a very important component in the design of application specific integrated circuits. This paper presents a novel low-power multiplexer-based 1-bit full adder that uses 12 transistors (MBA-12T). In addition to reduced transition activity and charge recycling capability, this circuit has no direct connections to the power-supply nodes, leading to a noticeable reduction in short-current power consumption. Intensive HSPICE simulation shows that the new adder has more than 26% in power savings over conventional 28-transistor CMOS adder and it consumes 23% less power than 10-transistor adders (SERF [1] and 10T [4]) and is 64% faster.

Index Terms—Full adder, low power, multiplexer, very large-scale integrated (VLSI) circuit.

I. INTRODUCTION

WITH THE EXPLOSIVE growth in laptops, portable personal communication systems, and the evolution of the shrinking technology, the research effort in low-power microelectronics has been intensified. Today, there are an increasing number of portable applications requiring small-area low-power high throughput circuitry. Therefore, circuits with low-power consumption become the major candidates [1]–[3] for design of microprocessors and system-components.

The 1-bit full adder is one of the most critical components of a processor, as it is used in the <AU: PLEASE SPELL OUT..?> (ALU), the floating-point unit, and address generation for cache or memory accesses [1]. A variety of full adders using static and dynamic logic styles have been reported in literature [1]–[8]. 34 of them have been found in [8] alone, including the most well-known static complementary CMOS adders using 28 transistors shown as Fig. 1(f) In [1], the static energy recovery full (SERF) adder shown in Fig. 1(b) is proposed, which requires only 10 transistors to implement a full adder as specified in Fig. 1(a). SERF has been shown to consume less power than a transmission function adder (TFA) [1]. In [4], some new full adders using 10-transistors have been proposed, shown as Fig. 1(c)–(e), named as 10T09A, 10T09B, 10T13A, respectively. These new 10-transistor adders are based on the same architecture shown in Fig. 1(a), using a novel 4-transistor XOR-XNOR gate.

In this paper, we propose a novel low-power multiplexer-based 1-bit full adder, named MBA-12T, that uses six iden-

tical multiplexers with 12 transistors in total. This new adder has low short-circuit current and reduced transition activity than previously proposed low-power adders. The MBA-12T adder is tested along with the 28-transistor complementary CMOS adder and four other low-power 10-transistor full adders [1], [4] using HSPICE [9]. The testing result shows that the MBA-12T consumes 26% less power than 28-transistor CMOS adder. Meanwhile, MBA-12T exhibits at least 23% in power-savings over the least power-consuming 10-transistor adder and a minimum of 64% in speed improvement over the fastest of all other tested adders.

The rest of this paper is organized as follows. In Section II, the new adder is proposed. In Section III, we present the simulation environment setup and the simulation results. Finally, Section IV concludes the paper.

II. NEW MULTIPLEXER-BASED FULL ADDER

A 1-bit full adder built upon six identical multiplexer gates is shown in Fig. 2. Substituting each of the multiplexer gates with a 2-transistor circuit (Fig. 2(b)) gives us the new MBA-12T adder, which requires a total of 12 transistors to realize the function of a full adder, shown in Fig. 3.

There are three major sources of power dissipation in a digital CMOS circuit: logic transition, short-circuit current and leakage current [6], [7]. The short-circuit current is the direct current passing through the supply and the ground, when both the NMOS and the PMOS transistors are simultaneously active [2], [6]. As the proposed MBA-12T adder does not have direct connections to V_{DD} or V_{SS} port (voltage connections to the back gate terminals are not considered), the probability of a direct path formation from positive voltage supply to the ground during switching can be substantially reduced; that is, the power consumption due to short circuit current is considered negligibly small. Furthermore, in the new MBA-12T adder, all of its internal gate nodes are directly excited by the fresh input signals (A , B , and C_{in}), leading to a much faster transition (low rise and fall times) in its output signals. As a result, the power consumption of the following buffer stage can benefit from faster/cleaner Sum and Cout outputs.

Similar to SERF, ADDER-10T09A, and 10T09B (Fig. 1), the new MBA-12T adder has the ability of reclaiming all the node charges during the discharging cycle of those nodes. Since the new MBA-12T uses 12 transistors, one can expect a modest increase of the internal node capacitances compared to SERF, 10T09A, 10T09B, and 10T13A adders (see Fig. 1). However, the switching activity of the MBA-12T adder will be considerably lower than that of previously proposed 10-transistor adders. That's because all of those adders (SERF and 10Ts) use an internally generated signal (A XNOR B) to control the output

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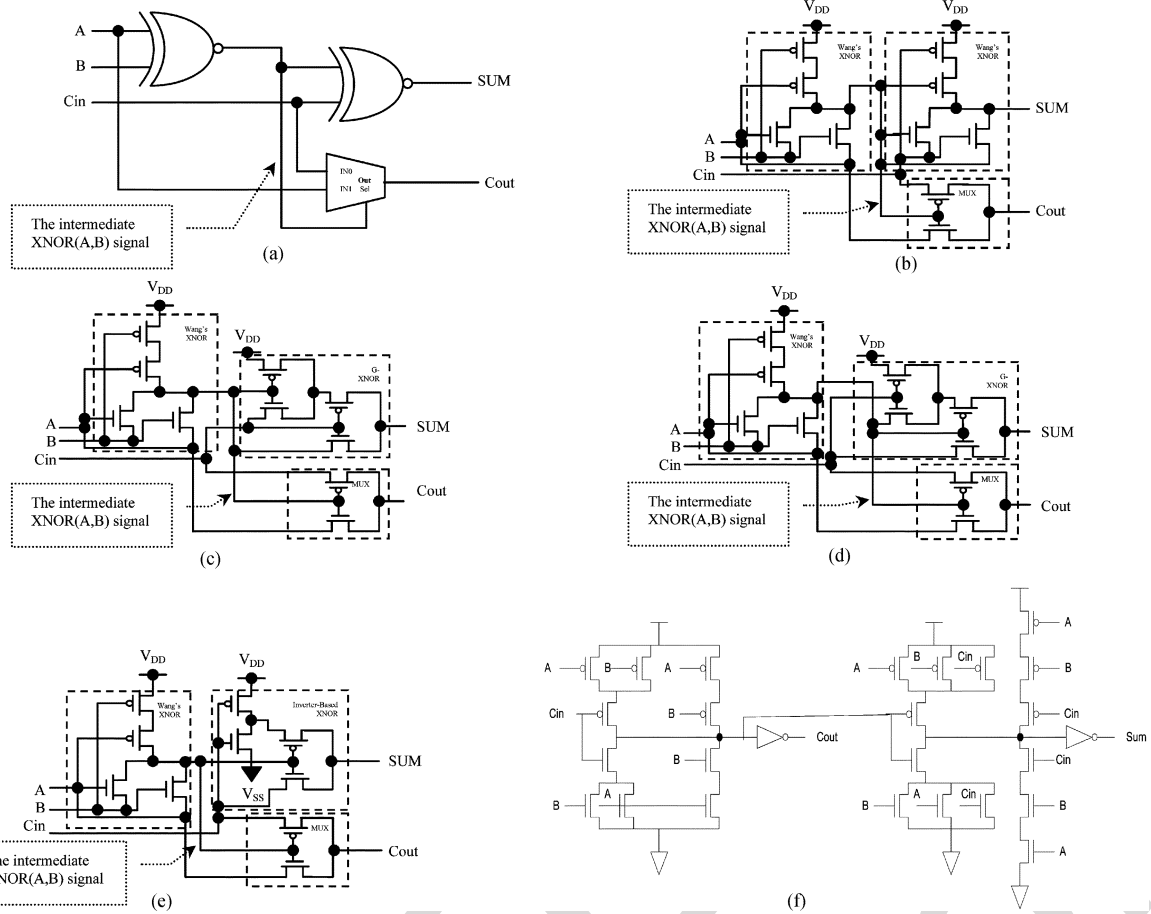


Fig. 1. Full adders. (a) Architecture. (b) SERF. (c) ADDER10T09A. (d) ADDR10T09B. (e) ADDR10T13A. (f) 28T CMOS.

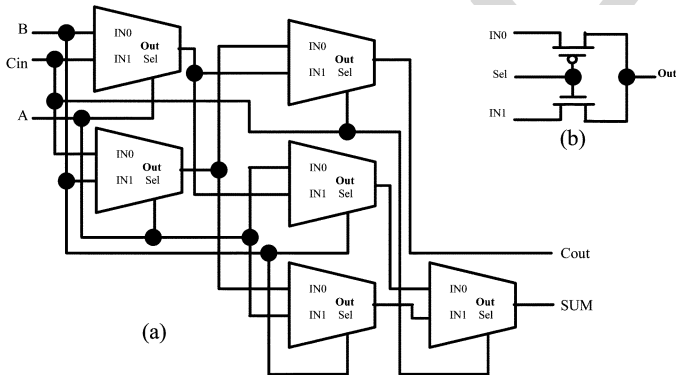


Fig. 2. (a) Architecture. (b) 2-T MUX.

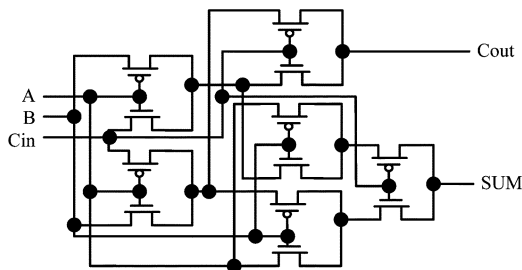


Fig. 3. New 12-Transistor adder.

transistor gates (four gates in total). Hence, the probability that

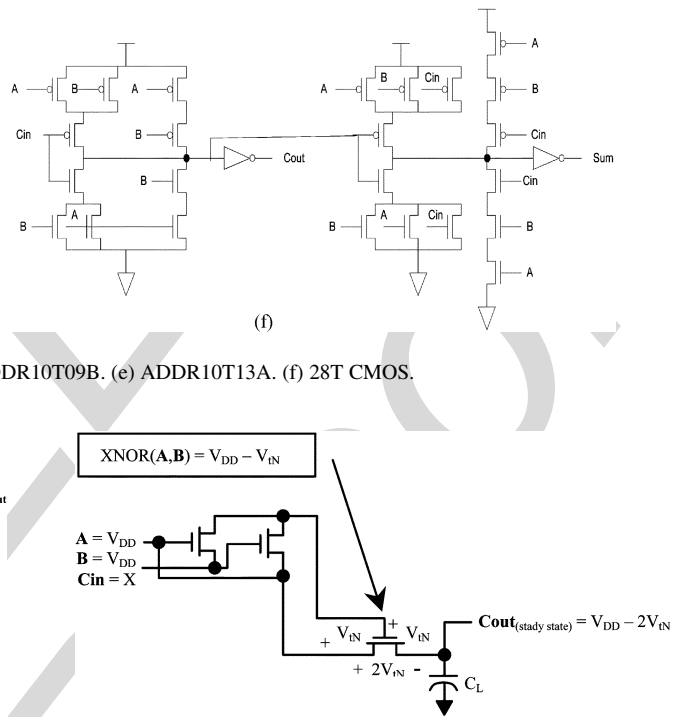


Fig. 4. Worst case logic "1" for SERF.

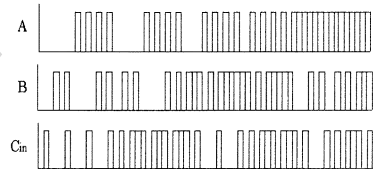


Fig. 5. Simulation input patterns.

a power-consuming transition (p_t) occurs is $\{p_{XNOR(A,B)} = 8/12 = 0.6667, p_t = [(6 \times (1/2) + 4 \times 0.6667)/10] = 0.5666\}$, i.e., at least 13.34% higher than that of the MBA-12T adder with switching probability calculated to be only 0.5: $\{p_i = 1/2, p_t = 12 \times (1/2)/12 = 0.5\}$.

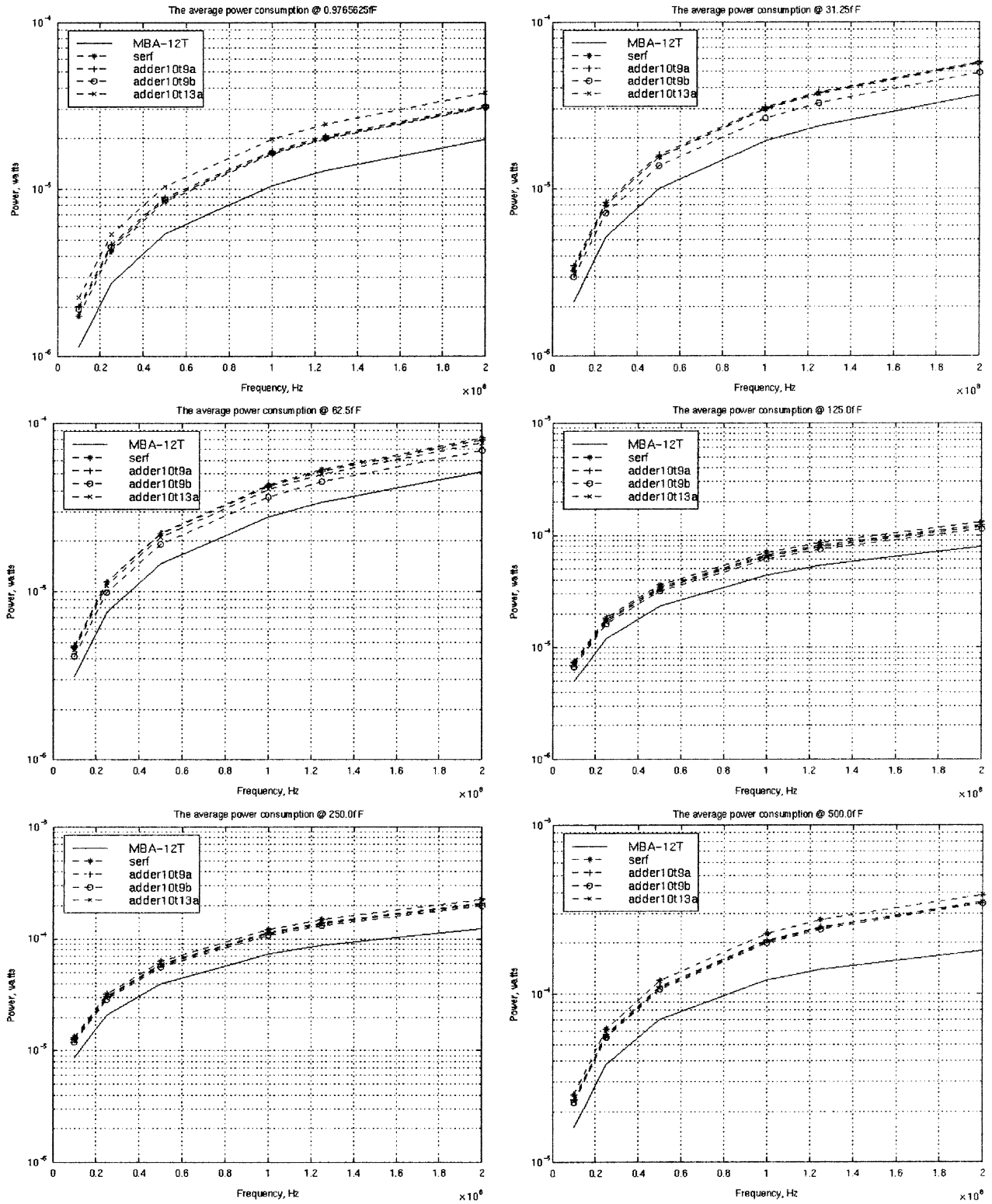


Fig. 6. Average power measurements.

Threshold loss problem [6] impacts the new adder only at its output nodes (Sum and C_{out}); that is, weak logic “1” can drop to $V_{DD} - V_{tN}$ and a worst case logic “0” equals to $|V_{tP}|$ volts. However, SERF will have a worst case logic “1” equal to $V_{DD} - 2V_{tN}$ at its C_{out} output port when, A and B are both equal to logic “1”, as shown in Fig. 4. Thus, the operational

supply voltage range for the SERF adder is limited to $V_{DD} > 2V_{tN} + |V_{tP}|$.

III. SIMULATION RESULTS

We have performed intensive simulations using HSPICE [9] on the new MBA-12T along with 28-transistor complementary

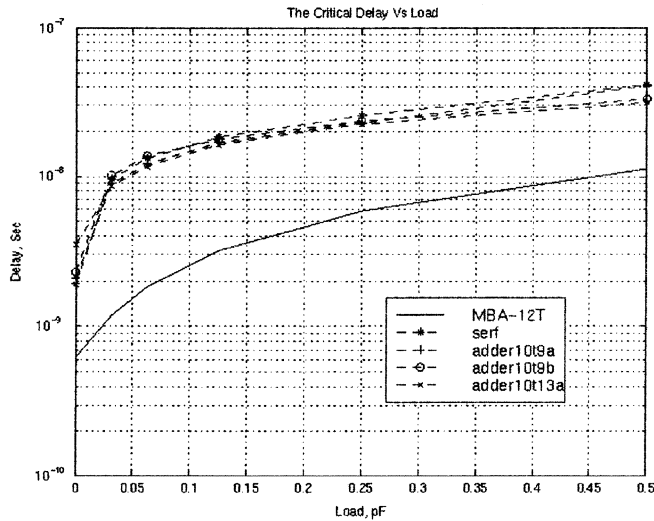


Fig. 7. Critical delay measurements versus load.

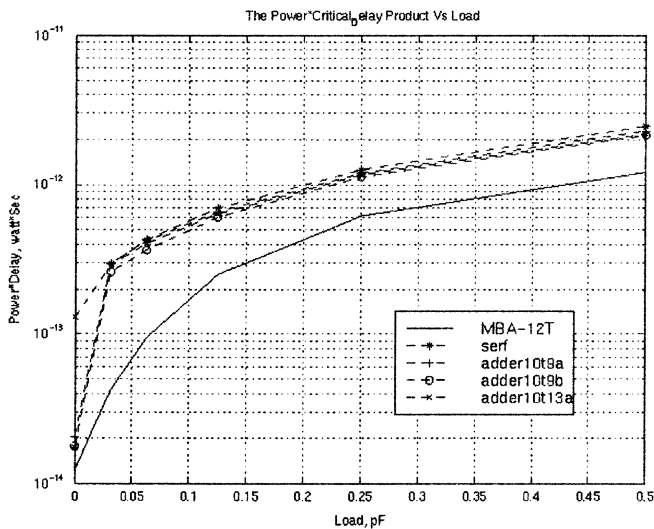


Fig. 8. Power * critical delay product versus load.

CMOS, SERF, 10T09A, 10T09B, and 10T13A adders shown in Fig. 1 at the schematic level under comparable simulation conditions. The technology being used is 0.35- μm CMOS digital technology (TSMC 35, Canadian Microelectronic Corporation) with a 3.3-V supply voltage. To establish an impartial testing environment, the simulations have been carried out using a comprehensive input signal pattern (Fig. 5), which covers every possible transition for a 1-bit full adder.

In our experiment, six frequencies (toggle rates) have been chosen for each input signal, swinging from 10 to 200 MHz. Also, six different loads (500 fF, 250 fF, 125 fF, 62.5 fF, 31.25 fF, and 0.976 562 5 fF) have been inserted to the output ports (Sum and C_{out}). In total, for each adder circuit, 36 HSPICE simulation runs (six frequencies by six loads) have been conducted.

Simulation results show that the new MBA-12T adder consumes at least 26% less power than that of the conventional 28-transistor complementary CMOS adder under all

above mentioned simulation conditions (Fig. 6). This is quite understandable as MBA-12T has much lower transistor count, thus much lower internal capacitance than 28-transistor CMOS adder. On average (calculated using arithmetic average), the new MBA-12T consumes 37.5%, 36.5%, 30.9%, and 36.3% less power than the respective SERF, 10T09A, 10T09B, and 10T13A. Thus, the ranking of those adders in terms of power savings will be as follows: MBA-12 is the first, 10T09B the second, 10T09A the third, 10T13A the fourth, and SERF the fifth.

The critical delay under various load conditions is presented in Fig. 7. The new MBA-12T, on average, exhibits a speed improvement by 78.9%, 78.2%, 78.4%, and 78.5% over SERF, 10T09A, 10T09B, and 10T13A, respectively. The critical delay of SERF, 10T09A, 10T09B, and 10T13A is determined by the C_{out} (not Sum signal) according to our simulation results.

Finally, the power-delay product of MBA-12T (Fig. 8), on average, is 59.7%, 60.1%, 55.9%, and 67.5% smaller than that of respective SERF, 10T09A, 10T09B, and 10T13A adders.

IV. CONCLUSION

In this paper, a novel low-power multiplexer-based 1-bit full adder (MBA-12T) is presented, which is constructed using 6 identical multiplexers and a total of 12 transistors. MBA-12T adder exhibits charge recycling capabilities and has very low short-circuit current. HSPICE simulations have been performed to evaluate MBA-12T and five other adders, including 28-transistor complementary CMOS, SERF and 10T adders. Simulation results show that MBA-12T consumes 26% less power than conventional 28-transistor CMOS adder. In addition, MBA-12T consumes 23% less power than the most power efficient 10-transistor adders and is 64% speedier than the fastest of all other tested adders. MBA-12T therefore, is suitable to be applied to build larger low-power high performance VLSI systems.

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