

# Edwin (Hsing-Mean) SHA

## **Professor**

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Edwin Sha received the B.S.E. degree in computer science and information engineering from National Taiwan University, Taipei, Taiwan, in 1986; he received the M.A. and Ph.D. degree from the Department of Computer Science, Princeton University, Princeton, NJ, in 1991 and 1992, respectively. From August 1992 to August 2000, he was with the Department of Computer Science and Engineering at University of Notre Dame, Notre Dame, IN. He served as the Associate Chair and the Graduate Director of the department at Notre Dame from 1995 to 2000. Since 2000, he has been a tenured full professor in the Department of Computer Science at the University of Texas at Dallas (UTD). He served as the Head of Computer Science Division in 2001 and the coordinator for Computer Systems Group at UTD.

He has published **more than 250** research articles in refereed international conferences and premier journals, including 70 journal articles (more than 30 IEEE and ACM Transactions papers). He served in the program committees and chairs of numerous international conferences and editors of many journals including IEEE Transactions on VLSI Systems, IEEE Transactions on Signal Processing, Journal of Embedded Computing, Journal of VLSI Signal Processing, etc. He received **Oak Ridge Association Junior Faculty Enhancement Award, Notre Dame CSE Teaching Award, NSF CAREER Award, NSF ITR grant, Microsoft Trustworthy Curriculum Award, NSFC Overseas Distinguished Young Scholar (B) and ChangJiang Scholar Honorary Chair Professorship (by Chinese ministry of education)**. He served as the program chairs or general chairs for many international conferences such as Great Lakes Symposium on VLSI (GLSVLSI) 1994, Parallel and Distributed Computing (PDCS) 2000, PDCS 2001, Parallel and Distributed Embedded Systems (PDES) 2005, Embedded and Ubiquitous Computing (EUC) 2006, Embedded Software Optimizations (ESO) 2006, EUC 2007, ESO 2007, International Symposium on Embedded Computing (SEC) 2008, ESO 2008, EM-Com 2009. His research has been supported by NSF (CAREER, ITR, EIA, IIS), Texas Instruments, AT&T, Texas Advanced Research Program, Microsoft Research, etc.

He has graduated 13 PhD students. Three of them received **UTD ECS Best PhD Dissertation Awards** in 2003, 2005 and 2007 respectively. His research goal is to efficiently design parallel, distributed and heterogeneous embedded architectures with the guarantee to satisfy the given requirements such as timing, power, memory-size, cost, security, etc. He has been developing new techniques that optimize timing performance and minimize power consumption for DSP applications and computer security applications considering multiple data memory modules and strict code-size constraint in embedded processors. Many optimization algorithms have been developed such as *hardware/software combined security defender, code-size reduction, multi-dimensional (MD) retiming, MD*

*rotation, MD interleaving, nest-loop pipelining, integrated design space minimization, fast intrusion detection hardware, and intelligent data/memory management and partitioning.* After moving to UTD, he has been studying efficient routing and partitioning in mobile ad-hoc networks. The detailed information can be found on the web at <http://www.utdallas.edu/~edsha>.

**Research Interests and Specialties**

Embedded Software and Systems, Computer and Network Security, Parallel Architectures and Systems, High-performance and Low-Power Real-Time Systems, Network Architectures, Compilers, Application Specific VLSI Design, Operating Systems, High-Level Synthesis.

**Citizenship:** USA

**Education**

Ph.D. Computer Science	Princeton University	Oct. 1992
Thesis title: Real-Time Fault Tolerance for Array Architectures		
Advisor: Prof. Kenneth Steiglitz		
M.A. Computer Science	Princeton University	Jan. 1991
B.S.E. Computer Science	National Taiwan University	June 1986
(GPA: 3.9/4.0, Book Coupon Awards, five times)		

**Professional Experience**

Aug. 00 - Present	Professor (Tenured)	Dept. of Computer Science University of Texas at Dallas, TX
Jan. 02 - Oct. 2004	Coordinator	Computer Systems Group University of Texas at Dallas, TX
Aug. 98 - Aug. 00	Associate Professor (Tenured) Associate Chair	Dept. of Computer Science & Engr. University of Notre Dame, IN
May 95 - Aug. 98	Assistant Professor Associate Chair	Dept. of Computer Science & Engr. University of Notre Dame, IN
Aug. 92 - May 95	Assistant Professor	Dept. of Computer Science & Engr. University of Notre Dame, IN
Sep. 88- July 92	RA and TA	Dept. of Computer Science Princeton University, NJ
Aug. 86- May 88	System Programmer	Marine Corps, Taiwan

**Membership**

ISCA, ACM and The Institute of Electrical and Electronics Engineers (IEEE).

## Courses taught and designed since August 1992

Computer and Network Security, Information Security, Parallel Architectures and Systems, Synthesis and Optimization of High-Performance Systems, Data Structures, VLSI Processor Arrays, Principles of Parallel Computing, Specialized Parallel Architectures, Operating Systems Principles, Automata.

## Graduate Students Advised (as their major thesis advisor)

1. Cathy Xu, **Ph.D. degree**, 2009, Ph.D. Dissertation Title: *Application Specific Interconnect Design And Scheduling on Multiprocessor Architectures.*
2. Jason Xue, **Ph.D. degree**, 2007, Ph.D. Dissertation Title: *Memory and Parallelism Optimization for Embedded Systems.* **Received the 2007 UTD ECS The Best PhD Dissertation Award.**
3. Meikang Qiu, **Ph.D. degree**, 2007, Ph.D. Dissertation Title: *Time and Power Optimization for Heterogeneous Parallel Embedded Systems.*
4. Meilin Liu, **Ph.D. degree**, 2006, Ph.D. Dissertation Title: *Loop Transformation Techniques Considering Timing and Memory Optimization for Embedded Systems.*
5. Kevin Chen, **Ph.D. degree**, 2006, Ph.D. Dissertation Title: *Efficient Network Architectures and Switch Fabrics for Packet Routing.*
6. Zili Shao, **Ph.D. degree**, 2005, Ph.D. Dissertation Title: *High Performance, Low Power and Secure Embedded Systems.* **Received the 2005 UTD ECS The Best PhD Dissertation Award.**
7. Bin Xiao, **Ph.D. degree**, 2003, Ph.D. Dissertation Title: *Dynamic Techniques for Constant Change Networks.*
8. Qingfeng Zhuge, **Ph.D. degree**, 2003, Ph.D. Dissertation Title: *Timing and Memory Optimization for Embedded Systems.* **Received the 2003 UTD ECS The Best PhD Dissertation Award.**
9. Timothy O'Neil, **Ph.D. degree**, 2002, Ph.D. Dissertation Title: *Techniques for Optimizing Loop Scheduling.*
10. Virgil Andronache, Master degree, 2000, Thesis Title: *Intelligent Page Placement and Replacement on Multiple Level Memory Systems.*
11. JiangFeng Ding, Master degree, 2000, Thesis Title: *Application Specific Image Compression for Virtual Conferencing.*
12. Fei Chen, Master degree, 2000, Thesis title: *Intelligent Algorithms for Hiding Memory Latencies.*
13. Joy Chantrapornchai, **Ph.D. degree**, 1999, Ph.D. Dissertation Title: *System Level Synthesis Considering Impreciseness Based on Fuzzy Theory.*
14. Sissadas Tongsima, **Ph.D. degree**, 1999, Ph.D. Dissertation Title: *Loop Scheduling for Applications with Fixed or Probabilistic Timing Information.*
15. Milind Saraph, Master degree, 1998, Thesis Title: *Distributed File Systems: An Empirical Study.*

16. David Surma, **Ph.D. degree**, 1998, Ph.D. Dissertation Title: *Collision Graph Based Communication Scheduling and Applications*.
17. Kaisheng Wang, Master Degree, 1998, Thesis Title: *Register Constrained Rotation Scheduling*.
18. Ted Zhihong Yu, Master Degree, 1997, Thesis Title: *Algorithms and Hardware Support for Multi-Dimensional Branch Anticipation*.
19. Michael Sheliga, **Ph.D. Degree**, 1997, Ph.D. Dissertation Title: *Efficient High Level Synthesis Using Hardware/Multi-Software Co-Design and Communication Minimization*.
20. Nelson Passos, **Ph.D. Degree**, 1996, Ph.D. Dissertation Title: *The Multi-Dimensional Retiming Framework*.
21. Nicole Sabine, Master Degree, 1995, Thesis Title: *Selectively Fault-Tolerant, Hard Real-Time Multiprocessor Scheduling*.
22. Yvonne (YuHong) Wang, Master Degree, 1995, Thesis Title: *Scheduling via Node Replication for Parallel Systems*.
23. Sissadas Tongsimma, Master Degree, 1995, Thesis Title: *Communication Sensitive Scheduling for Parallel systems*.
24. Jenny (QingYan) Wang, Master Degree, 1995, Thesis Title: *Memory Constrained Partitioning and Scheduling for Multi-dimensional Applications*.
25. John Swadener, Master Degree, 1994, Thesis Title: *A Simulation Environment for Automatic Partitioning and Scheduling of Parallel Programs Based on Simulated Annealing*.

#### **Undergraduate Students Advised**

1. Roger Patrick Gorman and Ronald Setia, 1999 and 2000, Research Project: *Java Parallel Virtual Machines*.
2. Sam Ruppert and Richard Wiseman, 1999 and 2000, Research Project: *Virtual Network Chat with Animated Face*.
3. Melissa Layton, Vincent Oh, 1999 and 2000, Research Project: *Virtual Mobile Dog: An example of Mobile Agent*.
4. Ronald Setia, Mohamed Helmy, and Roger Gorman, 1999, Research Project: *Simulator for Java Virtual Machine and Pipelined JVM*.
5. Ryan Carlson and Michael Dreznes, 1998 and 1999, Research Project: *Java Virtual Conference*.
6. Dominic Fahey and Clinton Grady, 1998 and 1999, Research Project: *Multiple-thread Real-Time Java Based Web Camera*.
7. Joseph Bishay and Donald Reinhart, 1997, Research Project: *Pegasus: tools for collaborating and communicating for multiple users*.
8. Nathan Isley, CSE, 1997, Research Project: *Virtual Friend based on Java*.
9. Becky Saydak, CSE, 1995, Research Project: *Real-Time Multiprocessor Scheduling for Fault-tolerance*.
10. Thomas Aranda, CSE, 1995, Research Project: *Simulation Tools for Parallel Systems*.

11. Dan Cieslak, CSE, 1995 and 1996, Research Project: *Efficient Parallel Programming*.

### Graduate Students being Currently Advised

1. Jingtong Hu, Ph.D. Student, Research Project: *Optimizations for Embedded Memory* .
2. John Tseng, Ph.D. Student, Research Project: *Optimal Memory Architectures for Multiple Cores*.
3. Cathy Xu, Ph.D. Student, Research Project: *Communication Minimization for Multi-Cluster Systems*.
4. Lei Zhang, Ph.D. Students, Research Project: *Data and Computation Replication to Minimize Scheduling* .
5. Yi He, Ph.D. Students, Research Project: *Intelligent Memory Scheduling* .
6. Dan Lorts, Ph.D. Students, Research Project: *Optimal Hiding of Communication on Multi-Processor Systems* .

### Grants

1. Oak Ridge Associated Universities, *Timing Optimization for Multi-Dimensional Scientific Applications*, Principal Investigator, \$10,000, June 1994 - May 1995.
2. NSF Cornell Theory Center, 90 service units for KSR and IBM SP1, Principal Investigator, August 1993 - January 1994.
3. NSF CAREER Award, *High-Level Design Methodologies for Time-Optimal and Memory-Optimal Systems*, Principal Investigator, MIPS 95-01006, \$139,000, (the amount from NSF), June 1995 - May 1999.
4. NSF Pittsburgh Supercomputing Center, 554 Service Units for Cray C90 and Cray T3D, Principal Investigator, September 1995 - September 1996.
5. NSF National Center for Supercomputing Applications, 25 SU Hours for CM5, Principal Investigator, August 1995 - January 1996.
6. NSF Cornell Theory Center, 100 service units for IBM SP2, Principal Investigator, August 1995 - January 1996.
7. NSF Equipment Grant, Principal Investigator, MIPS 95-01006, \$50,000, May 1996 - May 1999.
8. NSF, Co-PI (with Peter Kogge, Jay Brockman, Steven Bass, and Danny Chen), *Pursuing A Petaflop: Point Designs for 100 TF Computers Using PIM Technologies*, NSF ACS 96-12028, \$100,000, April 1996 - May 1997.
9. NSF, Co-PI (with Nelson Passos), *Architecture support and code generation for general nested loops with fine-grain parallelism*, MIP-9704276, \$240,000, July 1997 - June 2000.
10. DARPA ITO (through JPL and NASA), Co-PI (with Peter Kogge, Steven Bass, Jay Brockman, Andy Lumnsdaine and Vincent Freeh), *A Hybrid Technology MultiThreaded Architecture for Petaflops Computing*, JPL Award No. 961097, \$604,200, May 1997 - June 1999.
11. AT&T, PI, *Communication Bandwidth Reduce Techniques & IP video Phone*, Award No. A-98-11-00002, \$25,000, May 1998 - August 1999.

12. AT&T, PI, *Video Chat and Bandwidth Reduction Techniques*, \$25,000, September 1999 - May 2001.
13. Texas Instruments, PI, *Hardware/Software Co-Designs for DSP and Communications*, Lab. Equipments, \$49,514, November, 2000.
14. Xilinx, PI, *Embedded Systems Designs*, Lab. Equipments, \$43,390, January, 2001.
15. NSF, Co-PI (with I-L Yen, F. Bastani, Y. Deng, L. Khan), EIA-0103709, *A Distributed Component Repository for Rapid Synthesis of Adaptive Real-Time Systems*, \$499,866, September 2001 - August 2004.
16. ARP, PI, *Algorithms on High-Level Synthesis and Optimization for High-Performance Systems*, \$96,000, Jan. 2002 - Aug. 2004.
17. NSF, PI, CCR-0309461, *Design Space Exploration and Synthesis for Multiple-Mode Embedded Systems*, \$210,000 plus UTD Matching, Sept. 2003 - Aug. 2007, NSF ITR grant.
18. Microsoft, PI, *The Development of Trustworthy Computing Course*, \$50,000, Since Jan. 2005, Unrestricted gift account.
19. Hong Kong Polytech University, Academic Visiting Scholar Grant, HK\$30,000 plus travel expense, May 2004.
20. Wind River, PI, *Embedded Systems Research*, Wind River University Program Grant, Platform Software for Network Equipment, and Development tools for VxWorks, \$100,000, September 2004.
21. Altera Corporation, PI, *Embedded Systems Design and Optimization*, Altera University Program Grant, QUARTUS II development suites, \$26,170, Jan. 2005.
22. UTD, Co-PI (with W. Wu, F. Qiu), *Efficient Spatial-Temporal Analysis of Environment and Public Health Related Data*, \$60,000, May 2005 - Aug. 2006.
23. Hong Kong, Research Grant Council, CO-PI (with Bin Xiao), RGC PolyU A-PA2F, *To Provide Network Security from the Prevention of Buffer Overflows to the Early-stage Detection of DDoS Attacks*, HK \$150,000, Aug. 2005 - July 2007.
24. NSF, Co-PI (with W. Wu, F. Qiu), NSF IIS-0513669, *Efficient Spatial-Temporal Analysis of Environment and Public Health Related Data*, \$397,504, Sept. 2005 - Aug. 2008.
25. Hong Kong, Research Grant Council, Competitive Earmarked Research Grant (CERG), CO-PI (with Bin Xiao), CERG B-Q02S, *Early Detection and Effective Counteraction of DDoS attacks at the Victim Server Side*, HK \$534,000, Jan. 2007 - Dec. 2009.
26. Altera Corporation, PI, *Embedded Systems Education and Research*, Altera University Program Grant, QUARTUS II development suites, \$22,000, Dec. 2006.
27. NSFC, PI, NSFC-60728206, *Exploring Integrated Optimizations for Embedded Software on Parallel Systems*, Overseas Distinguished Young Scholar (B), National Natural Science Foundation of China, RMB\$440,000, 2008 - Present.
28. Hong Kong, Research Grant Council, Competitive Earmarked Research Grant (CERG), CO-PI (with Zili Shao), CERG B-Q60B, *Compiler-Assisted Scheduling Techniques for Energy Saving on Parallel Embedded Systems*, HK \$648,000, Jan. 2008 - Dec. 2010.
29. Hong Kong, Research Grant Council, Competitive Earmarked Research Grant (CERG), Co-PI (with Jason Xue), GRF 123609 (HK CityU 9041505), *Memory Access and Task Scheduling Optimization for Embedded Systems*, HK \$443,000, Sept. 2009 - Aug. 2012.

30. NSF, PI, *CPS: Synthesize Cyber Physical Systems Considering Uncertainties on Computation and Data Access Time*, \$330,010, Sept. 2009 - Aug. 2012, submitted.
31. NSF, PI, *CPS: Research: Optimization for Heterogeneous Cyber-Physical Systems* \$278,709, Sept. 2009 - Aug. 2012, submitted.

### Professional Activities and Awards

1. Microsoft Trustworthy Computing Curriculum Development Award, 2005.
2. Recently Invited Speeches:  
Hunan University, June 2009, Hunan University of Science and Technology, June 2009, Kunming University of Science and Technology, June 2009, Beihang University, July 2009, Capital Normal University, July 2009, Hunan University, July 2008, University of Electronic Science and Technology of China, July 2008, City University of Hong Kong, November 2007, University of Electronic Science and Technology of China, July 2007, Beihang University July 2007, Shanghai Jiaotong University, July 2007, Shandong University, July 2007, Renmin University of China, June 2006, Suzhou University, June 2006, Shandong University, June 2006, National Taiwan University, May 2006, Shandong University May 2005, Jiangsu University May 2005, Nanjing University December 2004, Zhejiang University December 2004, Jiangsu University December 2004, Shanghai Jiaotong University December 2004, Tsinghua University October 2004, National Taiwan University October 2004, Hong Kong Polytechnic University May 2004, Shanghai Jiaotong University May 2004, Tsinghua University March 2003.
3. Keynote/Distinguished Speeches:  
International Conference on Embedded Software and Systems, July 2008.  
Arizona State University, March 2007.  
2005 IFIP International Conference on Embedded And Ubiquitous Computing (EUC 2005), Nagasaki, Japan, December 2005.  
Emerging Information Technology Conference (EITC 2005), Taipei, Taiwan, August 2005.  
The Ninth Workshop on Compiler Techniques for High-Performance Computing, Taipei, Taiwan, March 2003.
4. **Overseas Distinguished Young Scholar (B)**, National Natural Science Foundation of China (NSFC), RMB\$400,000, 2007 - 2010.
5. **ChangJiang Scholar Honorary Chair Professorship**, Chinese Ministry of Education, 2009 - Present.
6. Member of Embedded Systems Expert Committee, Chinese Institute of Electronics, June 2006 - Present.
7. Guest (Honorary) Professor, Beihang University, Beijing China, 2009 - Present.
8. Visiting Professor, National Taiwan University, Taiwan, Sponsored by National Education Ministry, May 2006.
9. Specially Appointed Visiting Professor, Shandong University, Jinan, Shandong, China, 2006.
10. Guest (Honorary) Professor, Shandong University, Jinan, Shandong, China, 2005 - Present.
11. Part-Time PhD Advising Professor, Shandong University, Jinan, Shandong, China, 2006 - Present.

12. Guest (Honorary) Professor, Shanghai Jiaotong University, Shanghai, China, 2004 - Present.
13. Chair of the Judge Committee, The 4th National University Competition of Embedded System Design, (evaluating the 100 teams in the final list), Chinese Institute of Electronics, Beijing, China, October 2008.
14. Steering Committee Co-Chair of The Fourth International Conference on Embedded and Multimedia Computing (EM-Com 2009), Jeju, Korea, December, 2009.
15. General Committee Co-Chair of the 2008 International Workshop on Embedded Software Optimization (ESO 2008), Shanghai, China, December 2008.
16. General Committee Co-Chair of the 5th 2008 IEEE International Symposium on Embedded Computing (SEC 2008), Beijing, China, October 2008.
17. General Committee Co-Chair of the 2007 International Workshop on Embedded Software Optimization (ESO 2007), Taipei, Taiwan, December 2007.
18. General Chair of the 2007 IFIP International Conference on Embedded And Ubiquitous Computing (EUC 2007), Taipei, Taiwan, December 2007.
19. Steering Committee Chair of the International Workshop on Embedded Software Optimization (ESO).
20. Program Committee Chair of the 2006 IFIP International Conference on Embedded And Ubiquitous Computing (EUC 2006), Seoul, Korea, August 2006.
21. General Committee Co-Chair of the 2006 International Workshop on Embedded Software Optimization (ESO 2006), Seoul, Korea, August 2006.
22. General Committee Co-Chair of the First International Workshop on Security in Ubiquitous Computing (SecUbiq-05) in conjunction with EUC 2005, Nagasaki, Japan, Dec. 2005.
23. General Committee Co-Chair of the 1st International Workshop on Parallel and Distributed Embedded Systems (PDES) in conjunction with ICPADS 2005, Fukuoka, Japan, July 2005.
24. Evaluation Committee, The National Science and Technology Program for Systems-on-Chip (NSTPSoC), Republic of China, Taiwan, 2004.
25. Program Committee Chair of the 14th ISCA International Conference on Parallel and Distributed Computing Systems (PDCS), Texas, August 2001.
26. Program Committee Chair (with Prof. Ghulam M. Chaudhry) of the 13th ISCA International Conference on Parallel and Distributed Computing Systems (PDCS), Las Vegas, Nevada, August 2000.
27. **Teaching Award** of the Department of Computer Science and Engineering, University of Notre Dame, 1998.
28. Guest Editor, Special Issue on Embedded System Design & Optimization, *Journal of Embedded Computing (JEC)*, 2007 - 2008.
29. Guest Editor, Special Issue on Ubiquitous Computing, *International Journal on Pervasive Computing and Communications (JPCC)*, 2007 - 2008.

30. Guest Editor, Special Issue on Design and Programming of Signal Processors for Multimedia Communication, *Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology (JVLSI)*, 2007 - 2008.
31. Editor, *Journal of Embedded Computing (JEC)*, 2003 - Present.
32. Editor, *Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology (JVLSI)*, 2000 - Present.
33. Editor, *IEEE Transactions on Signal Processing*, handling submissions related to VLSI Systems and Programming Systems, 1999 - 2001.
34. Guest Editor (with Prof. Anantha Chandrakasan at MIT), Special Issue on low power VLSI systems, *IEEE Transactions on VLSI Systems*, published in Dec. 1998.
35. Editor, *Journal of Circuits, systems and Computers*, 1998.
36. NSF CAREER Award, *High-Level Design Methodologies for Time-Optimal and Memory-Optimal Systems*, 1995.
37. 1994 Junior Faculty Enhancement Award of Oak Ridge Associated University in Mathematics/Computer Science.
38. An Honorable alternate of 1993 Junior Faculty Enhancement Award of Oak Ridge Associated University in Mathematics/Computer Science.
39. International Advisory Board of the 4th International Conference on Information Security and Assurance (ISA 2010), India, June 2010.
40. International Advisory Committee of The 2009 International Conference on Security Technology (SecTech 2009), Jeju Island, Korea, December 2009.
41. Steering Committee of The 8th IEEE International Conference on Embedded Computing (EmbeddedCom-09), Dalian, China, September 2009.
42. Steering Committee and Panel Chair of the 2009 IFIP/IEEE International Conference on Embedded And Ubiquitous Computing (EUC 2009), Vancouver, Canada, August 2009.
43. Steering Committee of the 2009 The 6th IEEE International Conference on Embedded Software and Systems (ICCESS 2009), Hangzhou, Zhejiang, China, May 2009.
44. Steering Committee of the 2008 IFIP/IEEE International Conference on Embedded And Ubiquitous Computing (EUC 2008), Shanghai, China, December 2008.
45. International Advisory Committee of the 2008 International Conference on Security Technology (SecTech 2008), Hainan, China, December 2008.
46. International Advisory Committee of the IEEE 5th International Joint Conference on Computer Science and Software Engineering (JCSSE 2008), Kanchanaburi, Thailand, May 2008.
47. International Advisory Board of the International Conference on Information Security and Assurance (ISA 2008), Busan, Korea, April 2008.
48. International Advisory Committee of the 2007 international Workshop on Intelligent Systems and Smart Home (WISH 2007), Niagara Falls, Canada, August 2007.
49. Steering Committee of the International Workshop on Interactive Multimedia & Intelligent Services in Mobile and Ubiquitous Computing 2007 (IMIS2007), Seoul, Korea, April 2007.

50. Advisory Committee of the International Conference on Information Security and Computer Forensics (ISCF 2006), Chennai, India, December 2006.
51. Program Committee of the 2010 IEEE International Symposium on Parallel and Distributed Processing with Applications (ISPA 2010), Taipei, Taiwan, Sept. 2009.
52. Program Committee of 2010 International Conference on High Performance Computing & Simulation (HPCS), Caen, France, June, 2010.
53. Program Committee of the 7th Bi-Annual IFIP Conference on Distributed and Parallel Embedded Systems (DIPES), Brisbane, Australia, September 2010.
54. Program Committee of the 10th International Conference on Algorithms and Architectures for Parallel Processing (ICA3PP-2010), Busan, Korea, May 2010.
55. Program Committee of the 2009 Seventeenth International Conference on Advanced Computing and Communication (ADCOM 2009), Bangalore, India, December, 2009.
56. Program Committee of the 2009 IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS 2009), Grenoble, France, October 2009.
57. Program Committee of the The 7th IEEE/IFIP International Conference on Embedded and Ubiquitous Computing (EUC 2009), Vancouver, Canada, August, 2009.
58. Program Committee of the IEEE International Conference on Embedded Computer Systems: Architecture, Modeling and Simulation, (IC-SAMOS), Sammos, Greece, July 2009.
59. Program Committee of 2009 High Performance Computing and Simulation (HPC&S) Conference, Leipzig, Germany, June 2009.
60. Program Committee of the 2009 IASTED International Conference on Parallel and Distributed Computing and Networks (PDCN 2009), Innsbruck, Austria, Feb. 2009.
61. Program Committee of the The 10th International Conference on Computer Science & Informatics (CSI 2008), Shenzhen, China, December 2008.
62. Program Committee of the 2008 IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS 2008), Atlanta, Georgia, USA, October 2008.
63. Program Committee of the 6th Bi-Annual IFIP Conference on Distributed and Parallel Embedded Systems (DIPES 2008), Milano, Italy, September 2008.
64. Program Committee of the IEEE International Conference on Embedded Computer Systems: Architecture, Modeling and Simulation" (IC-SAMOS), Sammos, Greece, July 2008.
65. Program Committee of the 8th International Conference on Algorithms and Architectures for Parallel Processing (ICA3PP-2008), Cyprus, June 2008.
66. Program Committee of the 27th IEEE Real-Time Systems Symposium (RTSS 2007), Tucson, Arizona, December 2007.
67. Program Committee of the 19th IASTED International Conference on Parallel and Distributed Computing and Systems (PDCS 2007), Cambridge, Massachusetts, November 2007.
68. Program Committee of the 2007 IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS 2007), Salzburg, Austria, September 2007.

69. Program Committee of the Third International Symposium on Information Assurance and Security (IAS07), Manchester, United Kingdom, August 2007.
70. Program Committee of the IEEE International Conference on Embedded Computer Systems: Architecture, Modeling and Simulation" (IC-SAMOS), Sammos, Greece, July 2007.
71. Program Committee of the 7th International Conference on Algorithms and Architectures for Parallel Processing (ICA3PP-2007), Hangzhou, China, June 2007.
72. Program Committee of the 27th IEEE Real-Time Systems Symposium (RTSS 2006), Rio de Janeiro, Brazil, December 2006.
73. Program Committee of the 18th IASTED International Conference on Parallel and Distributed Computing and Systems (PDCS 2006), Dallas, Texas, November 2006.
74. Program Committee of 2006 IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS 2006), Seoul, Korea, October 2006.
75. Program Committee of the 5th Bi-Aannual IFIP Conference on Distributed and Parallel Embedded Systems (DIPES 2006), Braga, Portugal, October 2006.
76. Program Committee of the IEEE International Conference on Sensor Networks, Ubiquitous, and Trustworthy Computing (SUTC2006), Taichung, Taiwan, June 2006.
77. Program Committee of the 8th Asia Pacific Web Conference (APWeb), Harbin, China, January 2006.
78. Program Committee of the 17th IASTED International Conference on Parallel and Distributed Computing and Systems (PDCS 2005), Phoenix, Arizona, November 2005.
79. Program Committee of the 6th International Conference on Algorithms and Architectures for Parallel Processing (ICA3PP-2005), Melbourne, Australia, October 2005.
80. Program Committee of the 18th ISCA International Conference on Parallel and Distributed Computing Systems (PDCS), Las Vegas, NV, Sept. 2005.
81. Program Committee of Third IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS 2005), New York, New York, September 2005.
82. Program Committee of 2005 High Performance Computing and Simulation (HPC&S) Conference, Riga, Latvia, June 2005.
83. Program Committee of the First International Workshop on Security in Networks and Distributed Systems (SNDS 2005) in conjunction with ICPADS 2005, Fukuoka, Japan, July 2005.
84. Program Committee of Information Assurance and Security (IAS 2005), in conjunction with IEEE International Conference on Information Technology: Coding and Computing (ITCC 2005), Las Vegas, Nevada, April 2005.
85. Program Committee of The International Conference on Information Systems- New Generations (ISNG), Las Vegas, NV, April, 2005.
86. Program Committee of The First International Conference on Embedded Software and Systems (ICISS' 04), Hangzhou, China, Dec. 2004.
87. Program Committee of The International Conference on Information Systems- New Generations (ISNG), Las Vegas, NV, November, 2004.

88. Program Committee of the 16th IASTED International Conference on Parallel and Distributed Computing and Systems, MIT, Cambridge, MA, November, 2004.
89. Program Committee of the ACM/IEEE International Conference on Hardware/Software Codesigns and System Synthesis (CODES+ISSS 2004), Stockholm, Sweden, Sept., 2004.
90. Program Committee of the 17th ISCA International Conference on Parallel and Distributed Computing Systems (PDCS), San Francisco, CA, Sept. 2004.
91. Program Committee of The First International Workshop on Networked Embedded Computing (NEC 2004), in conjunction with The 2004 International Conference on Parallel Processing (ICPP 2004), Montreal, Canada, August, 2004.
92. Program Committee of The International Conference on Embedded and Ubiquitous Computing (EUC-04), Aizu, Japan, August, 2004.
93. Program Committee of 2004 High Performance Computing and Simulation (HPC&S) Conference, Magdeburg, Germany, June 2004.
94. Program Committee of Information Assurance and Security (IAS 2004), in conjunction with International Conference on Information Technology: Coding and Computing (ITCC 2004), Las Vegas, Nevada, April 2004.
95. Program Committee of the International Workshop of Embedded Computing (EC-04) in conjunction with the IEEE 24th International Conference on Distributed Computing Systems (ICDCS 2004), Tokyo, Japan, March 2004.
96. Program Committee of the 15th IASTED International Conference on Parallel and Distributed Computing and Systems, Marina del Rey, California, November, 2003.
97. Program Committee of the 2003 International Conference on Parallel Processing (ICPP 2003), Kaohsiung, Taiwan, October 2003.
98. Program Committee of the ACM/IEEE International Conference on Hardware/Software Codesigns and System Synthesis (CODES+ISSS 2003), Newport Beach, California, October 2003.
99. Program Committee of the 2003 The Seventh International Conference on Computer Science and Informatics (CSI 2003), Cary, North Carolina, September 2003.
100. Program Committee of The 2nd Workshop on Hardware/Software Support for Parallel and Distributed Scientific and Engineering Computing (SPDSEC 03), in conjunction with PACT-03, New Orleans, Louisiana, September 2003.
101. Program Committee of the 16th ISCA International Conference on Parallel and Distributed Computing Systems (PDCS), Reno, Nevada, August, 2003.
102. Program Committee of the 2003 International Symposium on Parallel Processing and Applications (ISPA 2003), Aizu-Wakamatsu City, Japan, July, 2003.
103. International Program Committee of 2003 High Performance & Large Scale Computing (HP&LSC) Conference, Nottingham, UK, June, 2003.
104. Program Committee of the 5th IEEE International Conference on Algorithms and Architecture for Parallel Processing (ICA3PP2002), Beijing, China, December 2002.
105. Program Committee of the 14th IASTED International Conference on Parallel and Distributed Computing and Systems, Cambridge, MA, November, 2002.

106. Program Committee of the 15th ACM/IEEE International Symposium on System Synthesis (ISSS 2002), Kyoto, Japan, October, 2002.
107. Program Committee of the Workshop on Embedded System Codesign, San Jose, California, September, 2002.
108. Program Committee of the 15th ISCA International Conference on Parallel and Distributed Computing Systems (PDCS), Louisville, Kentucky, September, 2002.
109. Program Committee of the 13th IASTED International Conference on Parallel and Distributed Computing and Systems, November, 2001.
110. Program Committee of the 4th IEEE International Conference on Algorithms and Architecture for Parallel Processing (ICA3PP2000), Hong Kong, December 2000.
111. Program Committee of the 12th IASTED International Conference on Parallel and Distributed Computing and Systems, Las Vegas, Nevada, November, 2000.
112. Program Committee of the 11th IASTED International Conference on Parallel and Distributed Computing and Systems, Cambridge, MA, November, 1999.
113. Program Committee of the IEEE Seventh International Symposium on the Frontiers of Massively Parallel Computation, Annapolis, Maryland, February, 1999.
114. Program Committee of the IEEE/ACM 11th International Symposium on System Synthesis (ISSS 1998), Hsinchu, Taiwan, December, 1998.
115. Program Committee of the 10th International Conference on Parallel and Distributed Computing and Systems, Las Vegas, Nevada, October, 1998.
116. Program Committee of the IEEE/ACM 10th International Symposium on System Synthesis, Antwerp, Belgium, September, 1997.
117. Program Committee of the IEEE Seventh Great Lakes Symposium on VLSI, Urbana, Illinois, March, 1997.
118. Program Committee of the IEEE/ACM Ninth International Symposium on System Synthesis, La Jolla, California, November, 1996.
119. Program Committee of the IEEE Sixth International Symposium on the Frontiers of Massively Parallel Computation, October, 1996.
120. Program Committee of the IEEE Sixth Great Lakes Symposium on VLSI, Ames, Iowa, March, 1996.
121. Program Committee of the IEEE Fifth Great Lakes Symposium on VLSI, Buffalo, New York, March, 1995.
122. Program Committee Co-Chair (with Prof. John Uhran) of the IEEE Fourth Great Lakes Symposium on VLSI, March, 1994, Notre Dame, Indiana. (Co-sponsored by IEEE Computer society, and IEEE Circuits and Systems Society and in cooperation with ACM).
123. Reviewer for Proposals submitted to NSF *Microelectronic systems Architecture* Program and *Design, Tool and Test* Program.
124. Reviewer for many journals including IEEE Transactions on VLSI Systems, IEEE Transactions on CAD, Journal of VLSI Signal Processing, IEEE Transactions on Circuits and Systems, IEEE Transactions on Parallel and Distributed Systems, IEEE Transactions on Signal Processing, etc.

## University Services

1. UTD Committee on Academic Integrity, University of Texas at Dallas, 2006 - 2009.
2. ECS CS Department Head Search Committee, University of Texas at Dallas, 2008 - Present.
3. ECS Dean's Advisory Committee on Continuity, ECS, University of Texas at Dallas, 2006 - Present.
4. School Personnel Review Committee, ECS, University of Texas at Dallas, 2004 - 2006.
5. Committee on Effective Teaching, University of Texas at Dallas, Representative member for ECS school, 2003 - 2005.
6. Coordinator, Computer Systems Group, Department of Computer Science, University of Texas at Dallas, Jan. 2002- 2004.
7. Committee on Academic Affairs, Erik Jonsson School of Engineering and Computer Science, University of Texas at Dallas, 2003 - 2005.
8. Committee on Effective Teaching, Erik Jonsson School of Engineering and Computer Science, University of Texas at Dallas, 2002 - 2005.
9. University Internal Research Committee, University of Texas at Dallas, 2002 - 2004.
10. Committee on Educational Policy, University of Texas at Dallas, August 2001 - August 2003.
11. Founding Director, *Hardware/Software Co-Design Lab for DSP and Communications*, University of Texas at Dallas, 2000.
12. Founding Co-director, *Computer and Network Architecture Lab*. University of Texas at Dallas, 2000.
13. Associate Chair of the Department of Computer Science, University of Texas at Dallas, May 2001 - Dec. 2001.
14. Chair, Ph.D. Degree Program Committee of the Department of Computer Science, University of Texas at Dallas, Sept. 2000 - August 2001.
15. **Associate Chair** of the Department of Computer Science and Engineering, University of Notre Dame, August 1995 - August 2000.
16. Graduate Committee of the Department of Computer Science and Engineering, University of Notre Dame, October 1992 - August 2000.
17. College Council, Engineering College, University of Notre Dame, August 1995 - May 1997.
18. Honesty Committee of the Department of Computer Science and Engineering, University of Notre Dame, August 1994 - August 2000.

## Patents

1. "Parallel Variable Length Pattern Matching Using Hash Table," C Xue, E. H.-M. Sha, M. Qiu, Q. Zhuge, U. S. Patent, Serial No. 11/307,864.

2. "Minimize Energy Consumption Using Optimal Voltage Assignment Algorithm," M. Qiu, E. H.-M. Sha, C. Xue, Q. Zhuge, U. S. Patent, Serial No. 11/307,924.

## Books, Book Chapters, Special Issues

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2. **Embedded and Ubiquitous Computing**, Tei-Wei Kuo, Edwin Sha, M. Guo, L. T. Yang, and Z. Shao, ISBN-10: 3-540-77091-7, Springer-Verlag, 2008.
3. **Embedded and Ubiquitous Computing**, Edwin Sha, S. Han, C. Xu, M. Kim, L. T. Yang, and B. Xiao, ISBN: 3-540-36679-2, Springer-Verlag, 2006.
4. M. Qiu and E. H.-M. Sha, "Power aware algorithm for heterogeneous wireless mesh network," Book Chapter in *Wireless Mesh Networking*, by George Aggelou, McGraw-Hill Professional, 2008.
5. M. Liu, Q. Zhuge, Z. Shao, C. Xue, M. Qiu and E. H.-M. Sha, "Optimizing Nested Loops with Loop Distribution and Loop Fusion," Book Chapter in *Embedded Systems: Status and Perspective*, American Scientific Publishers, 2007.
6. Special Issue on Embedded System Design & Optimization, *Journal of Embedded Computing (JEC)*, Guest Editor, 2007-2008.
7. **Recent Advances in Ubiquitous Computing**, *International Journal on Pervasive Computing and Communications (JPCC)*, Guest Editor, Vol. 4, No. 2, 2008.
8. Special Issue on Design and Programming of Signal Processors for Multimedia Communication, *Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology (JVLSI)*, Guest Editor, 2007 - 2008.
9. Special Issue on Low Power VLSI Systems, *IEEE Transactions on VLSI Systems*, Guest Editor, 1998.

## Refereed Publications

### Regular Journal Papers Published or Accepted for Publication

1. L. Zhang, M. Qiu, W. Tseng and E. H.-M. Sha, "Variable Partitioning and Scheduling for MPSoC with Virtually Shared Scratch Pad Memory," Published on line in *Journal of Signal Processing Systems*, April 2009, pp. 1 - 19.
2. Q. Xu, J. Xue, J. Hu and E. H.-M. Sha, "Optimizing Scheduling and Inter-Cluster Connection for Application-Specific DSP Processors," in *IEEE Transactions on Digital Signal Processing*, Vol. 57, No. 11, Nov. 2009, pp. 4538 - 4547.
3. K. Chen, S. Zhen and E. H.-M. Sha, "Fast and Noniterative Scheduling in Input-Queued Switches," in *International Journal of Communications, Network and System Sciences (IJCNS)*, Vol. 2, No. 3, June 2009, pp. 185-202.

4. M. Qiu and E. H.-M. Sha, "Cost Minimization while Satisfying Hard/Soft Timing Constraints for Heterogeneous Embedded Systems," in *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 14, No. 2, March 2009, pp. 25:01 - 25:30.
5. C. Xue, Z. Shao, M. Liu, M. Qiu and E. H.-M. Sha, "Optimizing Nested Loops with Iterational and Instructional Retiming," in *Journal of Embedded Computing (JEC)*, Vol. 3, Num. 1, 2009, pp. 29-37.
6. M. Qiu, M. Guo, C. Xue, L. T. Yang, E. H.-M. Sha and D. Charalampidis, "Loop Scheduling and Bank Type Assignment for Heterogeneous Multi-Bank Memory", Accepted in *Journal of Parallel and Distributed Computing (JPDC)*, Feb. 2009
7. K. Chen, S. Q. Zheng and E. H.-M. Sha, "Fast and Noniterative Scheduling in Input-Queued Switches: Supporting QoS," in *Computer Communications*, Vol. 32, No. 5, pp. 834-846, March 2009.
8. M. Qiu, L. T. Yang, Z. Shao, E. H.-M. Sha, "Dynamic and Leakage Energy Minimization with Soft Real-Time Loop Scheduling and Voltage Assignment," Accepted in *IEEE Transactions on Very Large Scale Integration Systems (IEEE TVLSI)*, December 2008.
9. C. Xue, Q. Zhuge, Y. He, M. Liu, and E. H.-M. Sha, "Variable Length Pattern Matching for Hardware Network Intrusion Detection System," Accepted in *Journal of Signal Processing Systems for Signal, Image, and Video Technology*, Sept. 2008.
10. Q. Zhuge, C. Xue, M. Qiu, J. Hu and E. H.-M. Sha, "Timing Optimization via Nest-Loop Pipelining Considering Code Size, " in *Journal of Microprocessors and Microsystems*, Vol. 32, No. 7, October 2008, pp. 351-363.
11. C. Xue, J. Hu, Z. Shao, and E. H.-M. Sha, "Iterational Retiming with Partitioning: Loop Scheduling with Complete Memory Latency Hiding," Accepted in *ACM Transactions on Embedded Computing Systems (ACM TECS)*, December 2007.
12. C. Xue, Z. Jia, Z. Shao, M. Wang and E. H.-M. Sha, "Optimized Address Assignment with Array and Loop Transformations for Minimizing Schedule Length," in *IEEE Transactions on Circuits and Systems I (IEEE TCAS)*, Vol. 55, No. 1, Feb. 2008, pp. 379 - 389.
13. Y. Shaih, Y. Hsu, C. Chen, C. Tseng and E. H.-M. Sha, " Adaptive Attenuation Factor Model for Localization in Wireless Sensor Networks," in *International Journal of Pervasive Computing and Communications*, Vol. 4, No. 3, Nov. 2008, pp. 257 - 267.
14. M. Qiu, E. H.-M. Sha, M. Liu, M. Lin, S. Hua, and L. T. Yang, "Energy Minimization with Loop Fusion and Multi-Functional-Unit Scheduling for Multidimensional DSP," in *Journal of Parallel and Distributed Computing (JPDC)*, Vol. 68, No. 4, April 2008, pp. 443-455.
15. B. Xiao, J. Cao, Z. Shao and E. H.-M. Sha, "An Efficient Algorithm for Dynamic Shortest Path Tree Update in Network Routing," in *Journal of Communications and Networks (JCN)*, Vol. 9, No. 4, Dec. 2007, pp. 499-510.
16. B. Xiao, J. Cao, Z. Shao, Q. Zhuge and E. H.-M. Sha, "Analysis and Algorithms Design for the Partition of Large-Scale Adaptive Mobile Wireless Networks," in *Computer Communications (Elsevier)*, Vol. 30, No. 8, June 2007, pp. 1899-1912.
17. Z. Jia, T. Liu, C Zhang and E. H.-M. Sha, "Markov Route Decision in Embedded Communication Middleware," in *ACTA Electronica Sinica*, Vol. 35, No. 7, July 2007, pp. 1228 - 1233.

18. K. Chen and E. H.-M. Sha, "Universal Routing and Performance Assurance for Distributed Networks," in *Journal of Interconnection Networks*, Vol. 8, No. 1, March 2007, pp. 1 - 28.
19. T. Liu, Z. Jia and E. H.-M. Sha, "Markov Finite Horizon Decision Algorithm of Shortest Path Tree," in *Computer Science (CCF Journal)*, ISDN 1002-137X, Vol 34, No. 8, Sept. 2007, pp. 266 - 270.
20. C. Xue, Z. Shao, and E. H.-M. Sha, "Maximizing Parallelism for Nested Loops via Loop Striping," in *Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology (JVLSI)*, Vol. 47, No. 2, May 2007, pp. 153 - 167.
21. Z. Shao, M. Wang, Y. Chen, C. Xue, M. Qiu, L. T. Yang and E. H.-M. Sha, "Real-Time Dynamic Voltage Loop Scheduling for Multi-Core Embedded Systems," in *IEEE Transactions on Circuits and Systems (IEEE TCAS)*, Vol. 54, No. 5, May 2007, pp. 445 - 449.
22. M. Qiu, C. Xue, Z. Shao, M. Liu and E. H.-M. Sha, "Energy Minimization for Heterogeneous Wireless Sensor Networks," Accepted in *Journal of Embedded Computing (JEC)*, No. 3, 2007.
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24. C. Chantrapornchai, W. Surakumpolthorn, and E. H.-M. Sha, "Design Exploration with Imprecise Latency and Register Constraints," in *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol 25, No. 12, Dec. 2006, pp. 2650 - 2662.
25. T. O'Neil and E. H.-M. Sha, "Time-Constrained Loop Scheduling with Minimal Resources," in *Journal of Embedded Computing (JEC)*, Vol. 2, No. 1, October 2006, pp. 103 - 117.
26. C. Xue, Z. Shao, Q. Zhuge, B. Xiao, M. Liu, and E. H.-M. Sha, "Optimizing Address Assignment for Scheduling DSPs with Multiple Functional Units," in *IEEE Transactions on Circuits and Systems (IEEE TCAS)*, Vol. 53, No. 9, September 2006, pp. 976 - 980.
27. Z. Shao, J. Cao, K. Chen, C. Xue, and E. H.-M. Sha, "Hardware/software Optimization for Array & Pointer Bound Checking Against Buffer Overflow Attacks," in *Journal of Parallel Distributed Computing (JPDC)*, Vol. 66, No. 9, September 2006, pp. 1129 - 1136.
28. Q. Zhuge, C. Xue, Z. Shao, M. Liu, M. Qiu and E. H.-M. Sha, "Design Optimization and Space Minimization Considering Timing and Code Size via Retiming and Unfolding," in *Journal of Microprocessors and Microsystems*, Vol. 30, Issue 4, June 2006, pp. 173-183.
29. Z. Shao, Q. Zhuge, M. Liu, C. Xue, E. H.-M. Sha and B. Xiao, "Algorithms and Analysis of Scheduling for Loops with Minimum Switching," in *International Journal of Computational Science and Engineering (IJCSE)*, Vol. 2, May 2006, pp. 88-97.
30. K. Chen and E. H.-M. Sha, "The Fat-Stack and Universal Routing in Interconnection Networks," in *Journal of Parallel and Distributed Computing (JPDC)*, Vol. 66, No. 5, May 2006, pp. 705-715.
31. Z. Shao, C. Xue, Q. Zhuge, M. Qiu, B. Xiao and E. H.-M. Sha, "Security Protection and Checking for Embedded System Integration Against Buffer Overflow Attacks via Hard-

- ware/Software,” in *IEEE Transactions on Computers (IEEE TC)*, Vol. 55, No. 4, April 2006, pp. 443 - 453.
32. Z. Shao, C. Xue, Q. Zhuge, B. Xiao and E. H.-M. Sha, “Loop Scheduling with Timing and Switching-Activity Minimization for VLIW DSP,” in *ACM Transactions on Design Automation of Electronic Systems (ACM TDAES)*, Vol. 11, No. 1, Jan. 2006, pp. 165 - 185.
  33. Z. Shao, Q. Zhuge, C. Xue and E. H.-M. Sha, “Efficient Assignment and Scheduling for Heterogeneous DSP Systems,” in *IEEE Transaction on Parallel and Distributed Systems (IEEE TPDS)*, Vol. 16, No. 6, June 2005, pp. 516-525.
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  41. E. H.-M. Sha, T. W. O’Neil and N. Passos, “Efficient Polynomial-time Nested Loop Fusion with Full Parallelism,” in *International Journal of Computers and Their Applications*, Vol. 10, No. 1, March 2003, pp 9-24.
  42. Z. Wang, E. H.-M. Sha and Y. Wang, “Partitioning and Scheduling DSP applications with Maximal Memory Access Hiding,” in *Eurasip Journal on Applied Signal Processing (EJASP)*, No. 9, September 2002, pp. 926-935.
  43. X. Hu, T. Zhou and E. H.-M. Sha, “Estimating Probabilistic Timing Performance for Real-time Embedded systems,” in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems (IEEE TVLSI)*, Vol. 9, Number 6, Dec. 2001, pp. 833-844.
  44. T. W. O’Neil, and E. H.-M. Sha, “Retiming Synchronous Data-Flow Graphs to Minimize Execution Time.” in *IEEE Transactions on Signal Processing (IEEE TSP)*, Vol. 49, Number 10, October 2001, pp. 2397-2407.

45. Z. Wang, T. W. O'Neil and E. H.-M. Sha, "Optimal Loop Scheduling for Hiding Memory Latency Based on Two Level Partitioning and Prefetching," in *IEEE Transactions on Signal Processing (IEEE TSP)*, Vol. 49, Number 11, November 2001, pp. 2853-2864.
46. Z. Wang, T. W. O'Neil and E. H.-M. Sha, "Minimizing Average Schedule Length under Memory Constraints by Optimal Partitioning and Prefetching," in *Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology (JVLSI)*, Vol. 27, Jan. 2001, pp. 215-233.
47. C. Chantrapornchai, E. H.-M. Sha, and X. S. Hu, "Efficient Module Selections for Finding Highly Acceptable Designs based on Inclusion Scheduling," in *Journal of Systems Architecture (JSA)*, Vol. 46, No. 11, 2000, pp. 1047-1071.
48. D. R. Surma, E. H.-M. Sha and P. M. Kogge, "Communication Reduction in Multiple Multicasts based on Hybrid Static-Dynamic Scheduling," in *IEEE Transactions on Parallel and Distributed Systems (IEEE TPDS)*, Vol. 11, No. 9, Sept. 2000, pp. 865-878.
49. C. Chantrapornchai, E. H.-M. Sha, and X. S. Hu, "Efficient Acceptable Design Exploration Based on Module Utility Selection," in *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol 19, No. 1, Jan. 2000, pp. 19-29.
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51. S. Tongsima, E. H.-M. Sha, C. Chantrapornchai, D. Surma and N. Passos, "Probabilistic Loop Scheduling for Applications with Uncertain Execution Time," in *IEEE Transactions on Computers (IEEE TC)*, Vol. 49, No. 1, Jan. 2000, pp. 65-80.
52. S. Tongsima, T. W. O'Neil, C. Chantrapornchai and E. H.-M. Sha, "Properties and Algorithms for Unfolding of Probabilistic Data-flow Graphs," in *Journal of VLSI Signal Processing (JVLSI)*, Vol. 25, No. 3, July 2000, pp. 215-234.
53. E. H.-M. Sha, and C. Chantrapornchai, "Optimizing Page Replacement for Multiple-Level Memory Hierarchy," (regular paper) in *International Journal of Computers and Their Applications*, Vol. 6, No. 4, Dec. 1999, pp. 212-222.
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55. S. Tongsima, E. H.-M. Sha, C. Chantrapornchai, and N. Passos, "Efficient Loop Scheduling and Pipelining for Applications with Non-uniform Loops," (regular paper) in *IASTED International Journal of Parallel and Distributed Systems and Networks*, Vol. 1, No 4, 1998, pp. 204-211.
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57. D. R. Surma and E. H.-M. Sha, "Collision Graph based Communication Scheduling for Parallel Systems," (regular paper) in *International Journal of Computers and Their Applications (IJCTA)*. Vol. 5, No. 1, March 1998, pp. 11-22.

58. L.-F. Chao and E. H.-M. Sha, "Scheduling Data-Flow Graphs via Retiming and Unfolding," (regular paper) in *IEEE Transactions on Parallel and Distributed Systems (IEEE TPDS)*, Vol. 8, No. 12, December 1997, pp. 1259-1267.
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61. L.-F. Chao, E. H.-M. Sha and A. LaPaugh, "Rotation Scheduling: A Loop Pipelining Algorithm," (regular paper) in *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 16, No. 3, March 1997, pp. 229-239.
62. N. Passos, E. H.-M. Sha and L.-F. Chao, "Multi-Dimensional Interleaving for Synchronous Circuit Design Optimization," (regular paper) in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 16, No. 2, February 1997, pp. 146-159.
63. Q. Wang, E. H.-M. Sha and N. Passos, "Optimal Data Scheduling for Uniform Multi-dimensional Applications," *IEEE Transactions on Computers (IEEE TC)*, Vol. 45, No. 12, December 1996, pp. 1439-1444.
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65. M. Sheliga and E. H.-M. Sha, "Hardware/Software Co-design With the HMS Framework," (regular paper) in *Journal of VLSI Signal Processing Systems (JVLSI)*, Vol. 13, No. 1, August 1996, pp. 37-56.
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68. L.-F. Chao and E. H.-M. Sha, "Static Scheduling for Synthesis of DSP Algorithms on Various Models," (regular paper) in *Journal of VLSI Signal Processing (JVLSI)*, Vol 10, 1995, pp 207-223.
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### Submitted Journal Papers Waiting for Review Decision

72. J. Hu, C. Xue, M. Qiu, W. Tseng and E. H.-M. Sha, "Minimize Data Transfer for Reprogramming on Wireless Sensor Network," submitted to *Journal of Parallel and Distributed Computing (JPDS)*
73. L. Zhang, M. Qiu, W. Tseng and E. H.-M. Sha, "Performance and Energy Optimal Scheduling for DSP Processor with Multi-Module Memory," submitted to *IEEE Transactions on Consumer Electronics*.
74. C. Xue, Q. Zhuge, Z. Shao, M. Qiu and E. H.-M. Sha, "Maximize Parallelism for Nested Loops with Iterational and Instructional Retiming," submitted to *IEEE Transactions on Parallel and Distributed Systems*.
75. M. Liu, Q. Zhuge, Z. Shao, C. Xue and E. H.-M. Sha, "General Loop Fusion Technique with Improved Timing Performance and Minimal Code Size," submitted to *IEEE Transactions on Computers*.
76. M. Liu, Q. Zhuge, Z. Shao and E. H.-M. Sha, "Efficient Loop Fusion for Two-level Loops Considering Timing and Code Size," submitted to *Journal of Embedded Computing*.
77. Z. Wang and E. H.-M. Sha, "Multiple Loop Nests Scheduling by Integrating Loop Partitioning and Data Padding," submitted to *ACM Transactions in Embedded Computing Systems*.
78. T. W. O'Neil, S. Tongsima, and E. H.-M. Sha, "Extended Retiming: Transforming Data-Flow Graphs to Minimize Clock Period," submitted to *International Journal of Computers and Their Applications*.

### Refereed Conference Papers

79. Y. He, C. Xue, C. Xu and E. H.-M. Sha, "Co-Optimization of Memory Access and Task Scheduling on MPSoC Architectures with Multi-Level Memory," in *Proc. The 15th IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC 2001)*, Taipei, Taiwan, Jan. 2010.
80. C. Xu, C. Xue, Y. He, E. H.-M. Sha, "Energy Efficient Joint Scheduling and Multi-core Interconnect Design," in *Proc. The 15th IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC 2001)*, Taipei, Taiwan, Jan. 2010.
81. M. Qiu, G. Wu, C. Xue, J. Hu, W. Tseng, and E. H.-M. Sha, "Energy Minimization and Latency Hiding for Heterogeneous Parallel Memory Modules," in *Proc. The IEEE Fifteenth International Conference on Parallel and Distributed Systems (ICPADS 2009)*, Shenzhen, China, Dec. 2009.
82. J. Hu, C. Xue, W. Tseng, M. Qiu, Y. Zhao, and E. H.-M. Sha, "Minimizing Memory Access Schedule for Memories with Single or Dual Controller," in *Proc. The IEEE Fifteenth International Conference on Parallel and Distributed Systems (ICPADS 2009)*, Shenzhen, China, Dec. 2009.
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