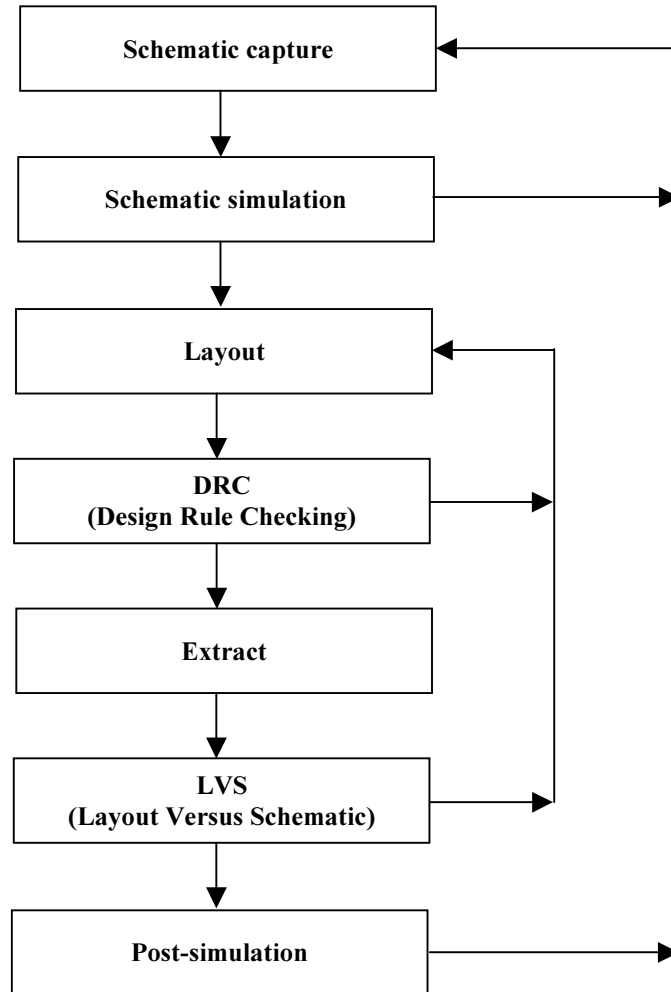


This tutorial is for layout with virtuoso in Cadence, before you begin the layout, you should have already done the following:

1. Drawing and successfully simulated the circuit in schematic level.
2. Have setup the environment for MOSIS cmosp35.3.0 kit.

The design flow,



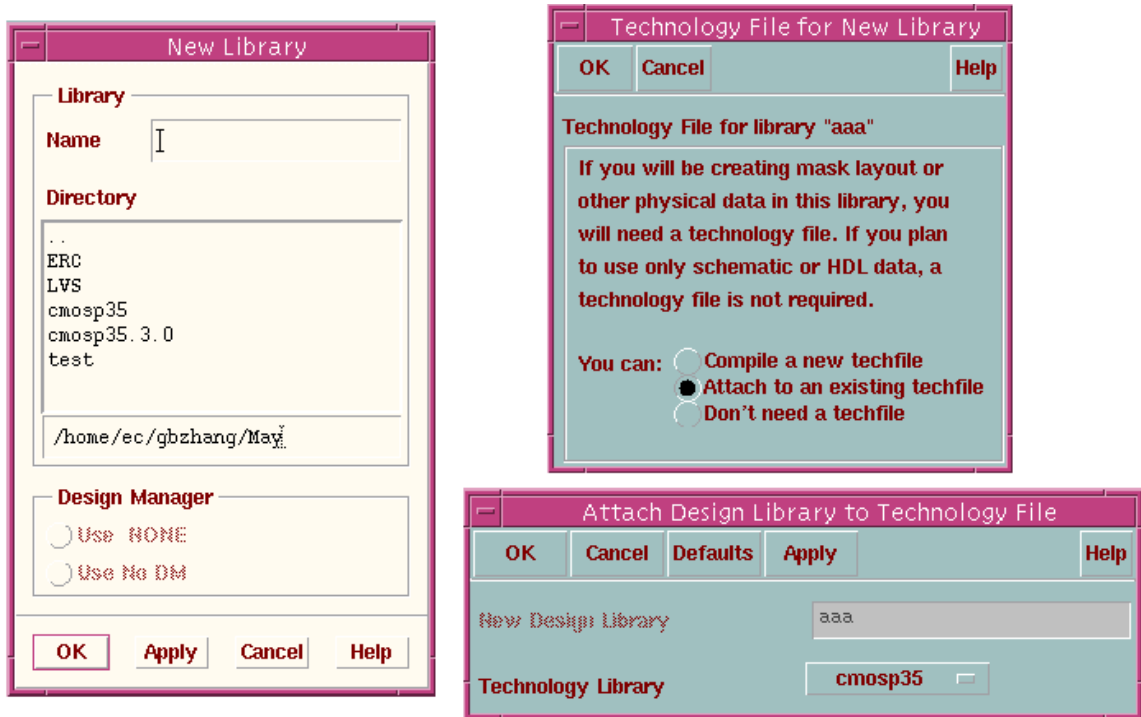
Schematic capture and simulation

Please refer to:

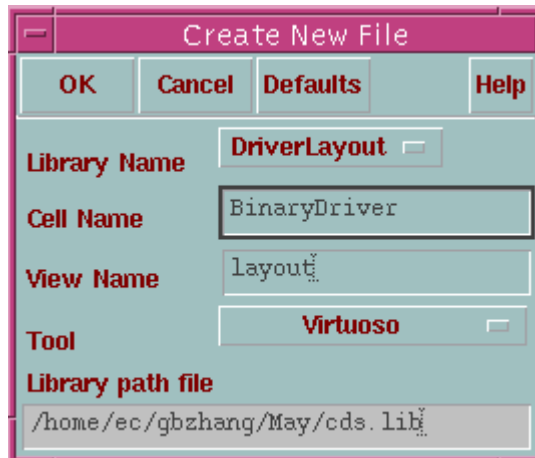
<http://www.utdallas.edu/~linxf/cadence.html>

Layout

1. Create library for layout using tsmc35 technology.
In the windows of "Library Manager" from icfb menu, choose file/new/library, input a library name you like and then press "ok".
Then select "attach to a existing technology file", later on choose "cmosp35" as the technology file library then confirm.



2. Create a new cellview in layout type with the same name of the correspondent schematic cellview in Library manager.



3. Draw the layout using virtuoso. You can learn more details of drawing layout by using online menu “*Openbook*”. Start a new terminal window and type

Openbook menu &

Select section:

Custom IC and deep sub-micron Design / Custom IC Layout / Layout / Cells design tutorial

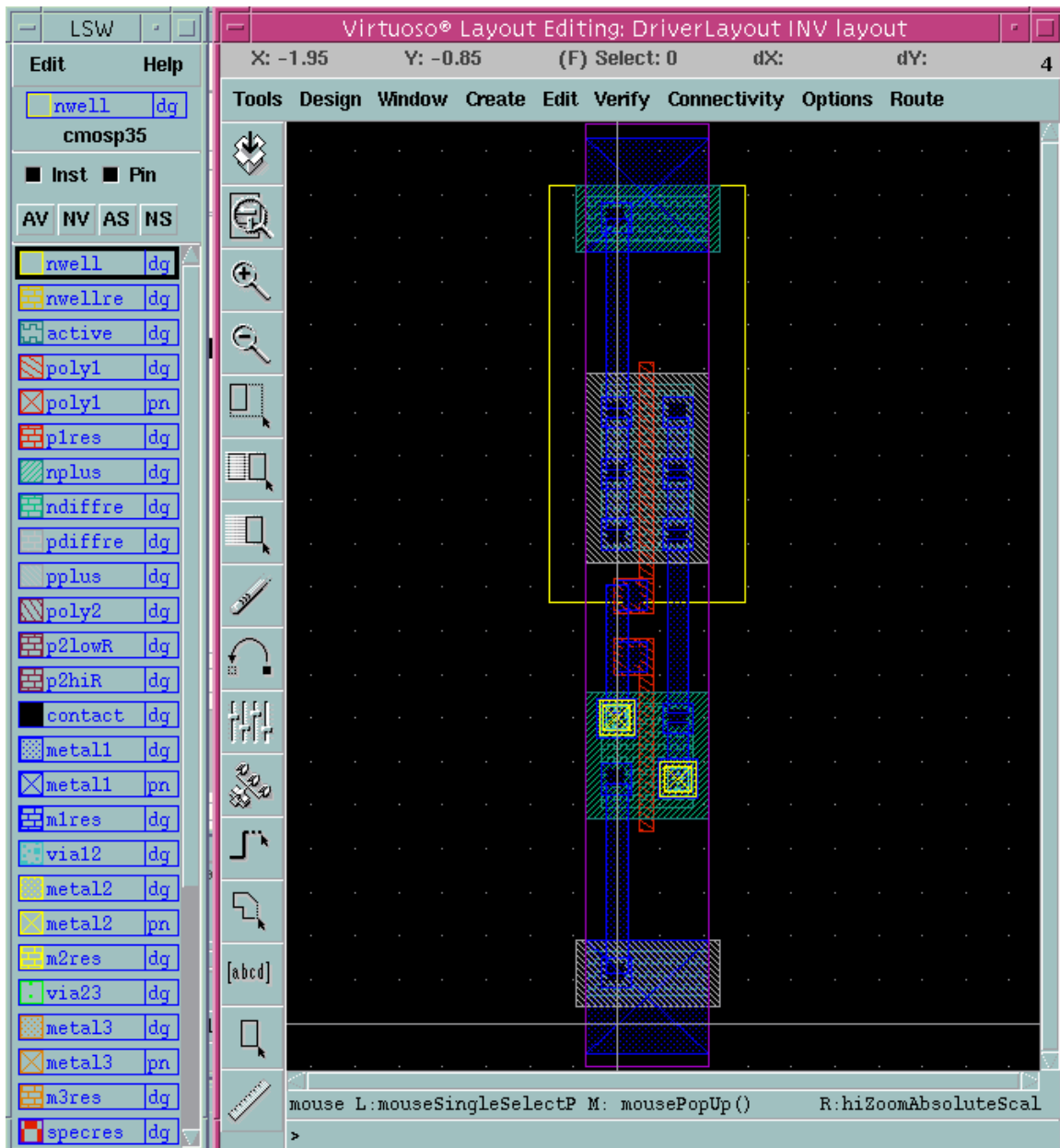
Following is an example of an inverter layout.

Basic commands used in drawing the inverter layout is listed below.

1. Click on the LSW window to change the drawing layer.
2. Left click : select object
3. r : create a rectangle
4. Shift-z : zoom out.
5. Control-z: zoom in.
6. s : stretch
7. Delete : delete object

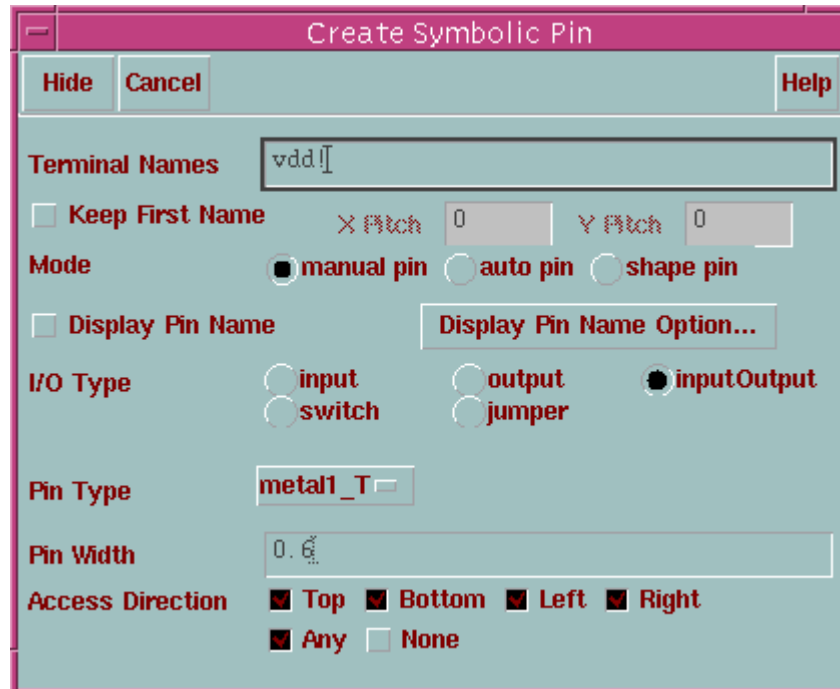
Basic layers used in drawing the inverter layout:

nwell, poly1, nplus, pplus, active, metal1, contact,



Create pins:

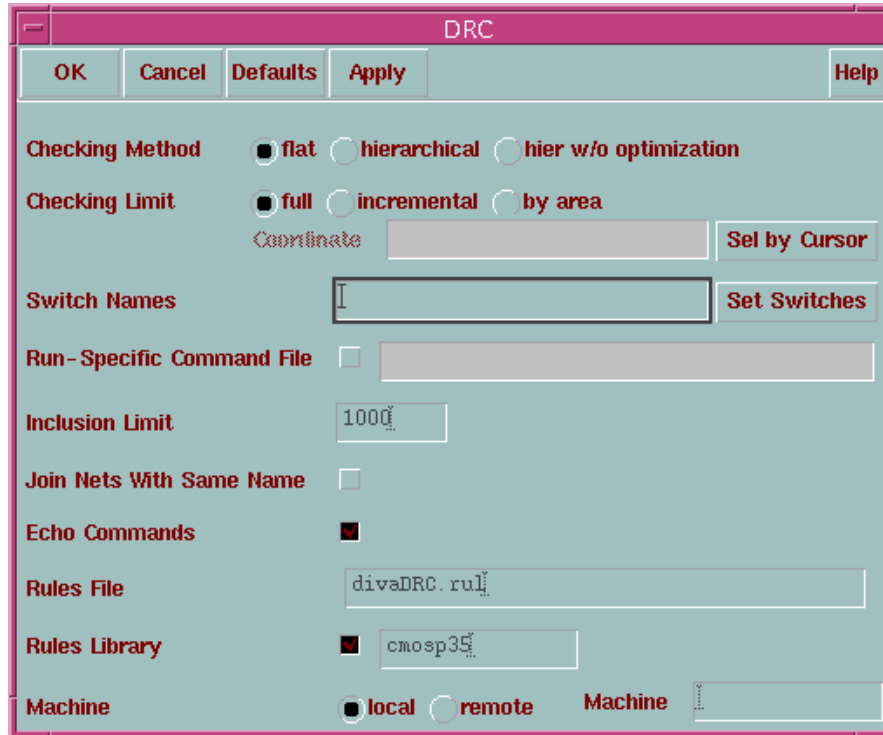
To connect the layout cellview to other parts of the circuits, we need to define the input or output pins of the cellview. This is the same as which is defined in schematic and the component symbol. Besides, the pin names in the layout should exactly match with the pin names in the schematic and symbol. The basic method to use menu command: *create/pin*



You can also use “*Create/Label*” to generate a label on the point where you want to add a pin, and then use “*Create / Pins from labels*” to generate pins. Make sure to set correct

DRC (Design Rule Checking)

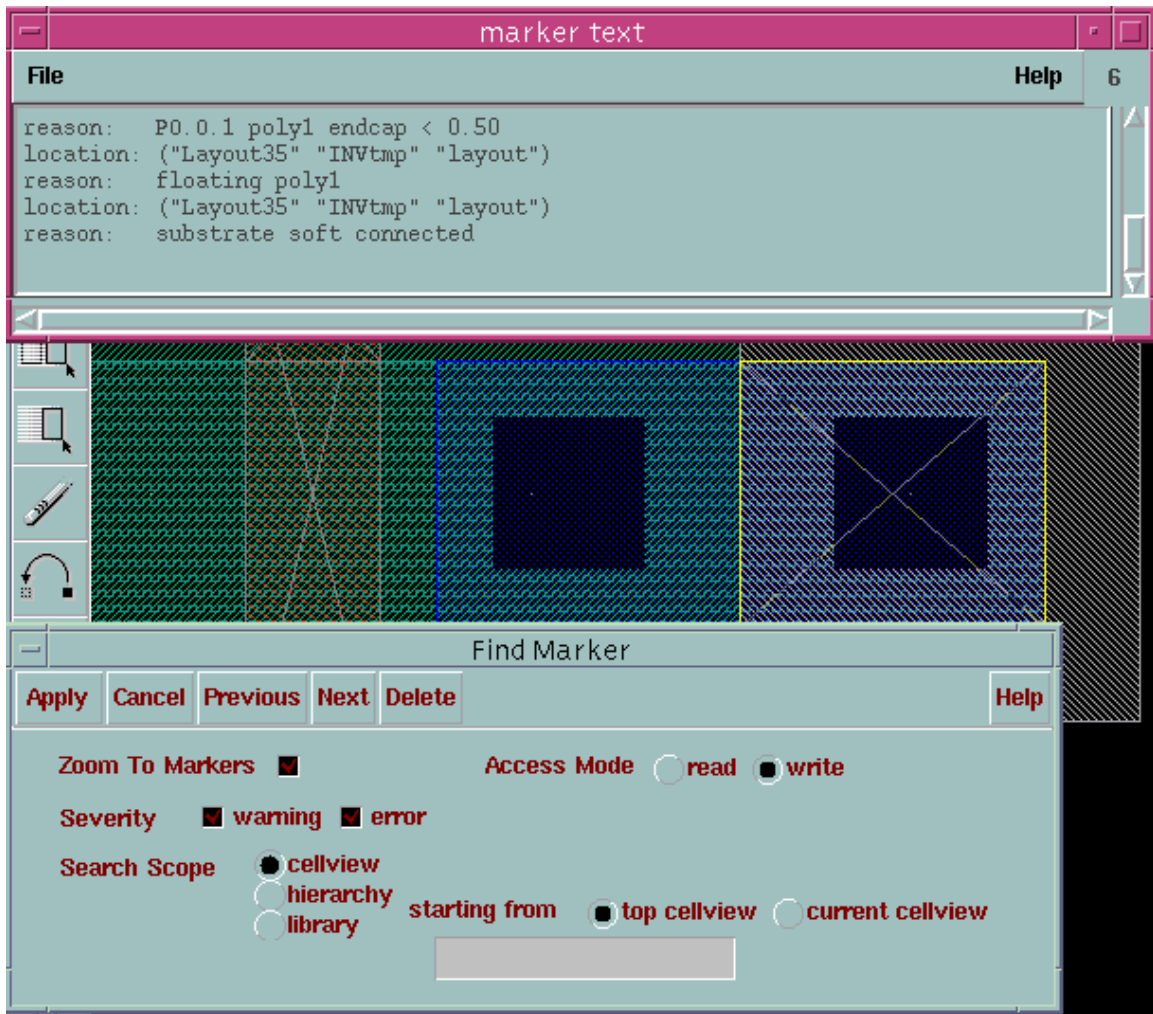
For any semiconductor process, the layout should obey all the design rules provided by the manufacturer. To check the layout design rules, use menu command: *verify/DRC*



Normally, there will be some errors when firstly run a DRC check. Look at the icfb window message to find the errors and correct them on the layout.

```
DRC started.....Mon Jun  4 12:28:48 2001
completed ...Mon Jun  4 12:28:56 2001
CPU TIME = 00:00:02  TOTAL TIME = 00:00:08
***** Summary of rule violation for cell "INVtmp layout" *****
# errors  Violated Rules
1  nohmic region without a contact
2  M1.W.1 metall width < 0.50
4  floating poly1
4  CO.C.1 active contact to gate spacing < 0.30
8  floating contact
2  CO.E.1 active overlap of contact < 0.15
8  M1.E.1 metall enclosure of cont < 0.15
2  NP.C.6/PP.C.6 butt implants from different nets
4  CO.W.1 contact width != 0.40
1  CO.E.4 nplus overlap of contact < 0.25
1  pohmic region without a contact
1  CO.E.3 pplus overlap of contact < 0.25
2  OD.C.3 ndiff spacing to hot nwell < 2.60
8  PO.0.1 poly1 endcap < 0.50
3  substrate soft connected
51 Total errors found
```

To locate the specific position of an layout error, use menu command: *Verify/Markers/Find*



The reasons for the error will be displayed on the "marker text" window, thus make it easy for users to correct the errors.

Extraction

After correct all the layout errors, you can extract the layout to view type of “*extracted*” by using menu command: *Verify / Extract*

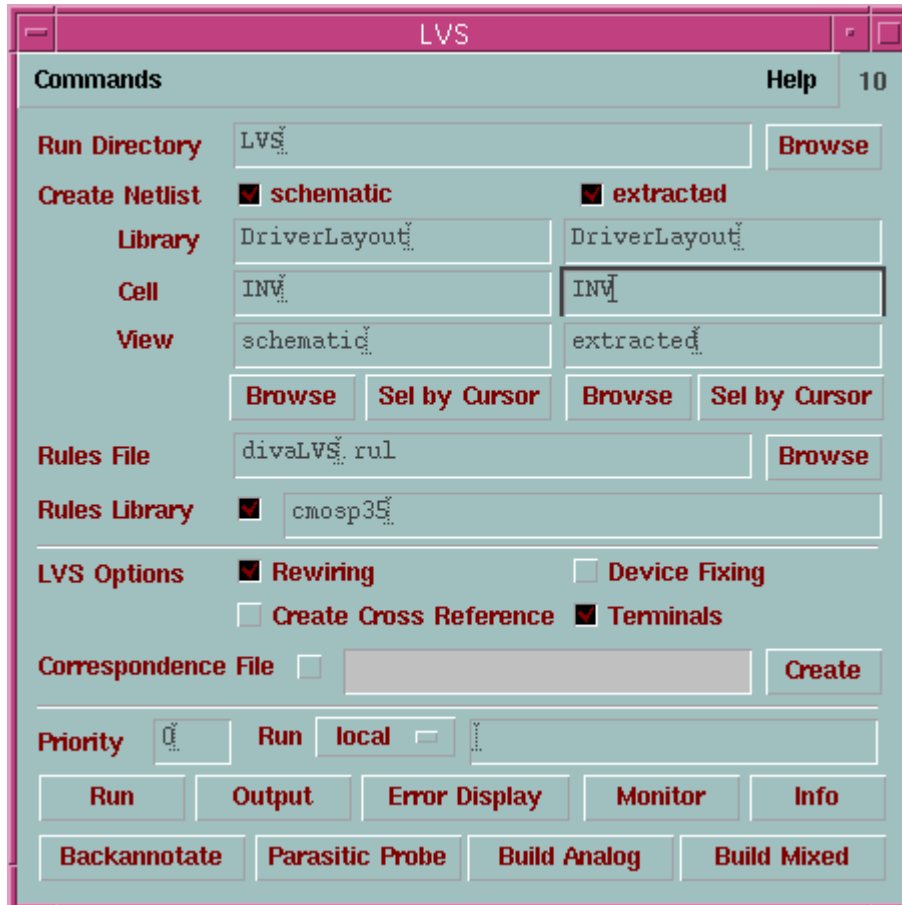
The screenshot shows the 'Extractor' dialog box with the following settings:

- Extract Method:** flat, macro cell, full hier, incremental hier
- Join Nets With Same Name:**
- Echo Commands:**
- Switch Names:** [Empty text box] **Set Switches** [Button]
- Run-Specific Command File:** [Empty text box]
- Inclusion Limit:** [Text box containing 1000]
- View Names:** **Extracted** [Text box containing extracted], **Excell** [Text box containing excell]
- Rules File:** [Text box containing divaEXT.rul]
- Rules Library:** [Text box containing cmosp35]
- Machine:** local, remote, **Machine** [Empty text box]

The extracted view of the layout can be used in simulation as the schematic, which will be described in post-simulation section.

LVS (Layout Versus Schematic)

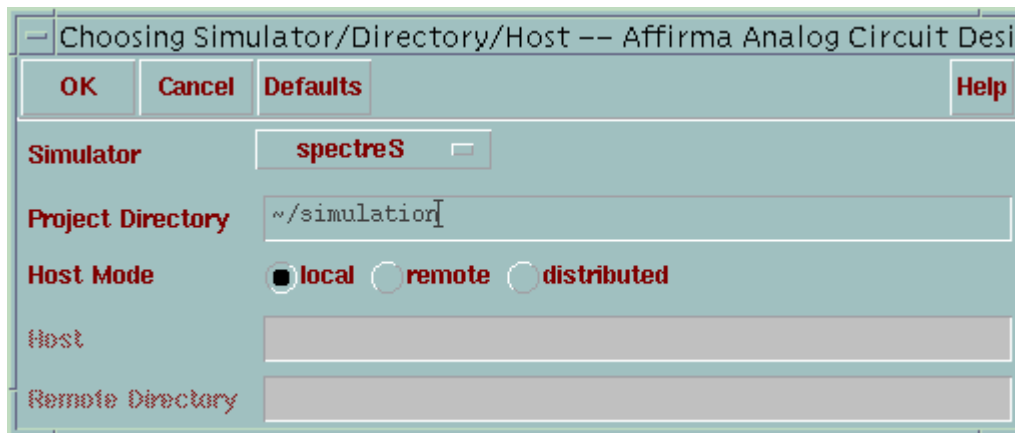
LVS is to verify if the layout is a restrict explanation of the schematic. It is very helpful when there's hidden errors in the layout and we need to find the difference and correct them. Use the menu command: *Verify / LVS...* to start up the *LVS* form.



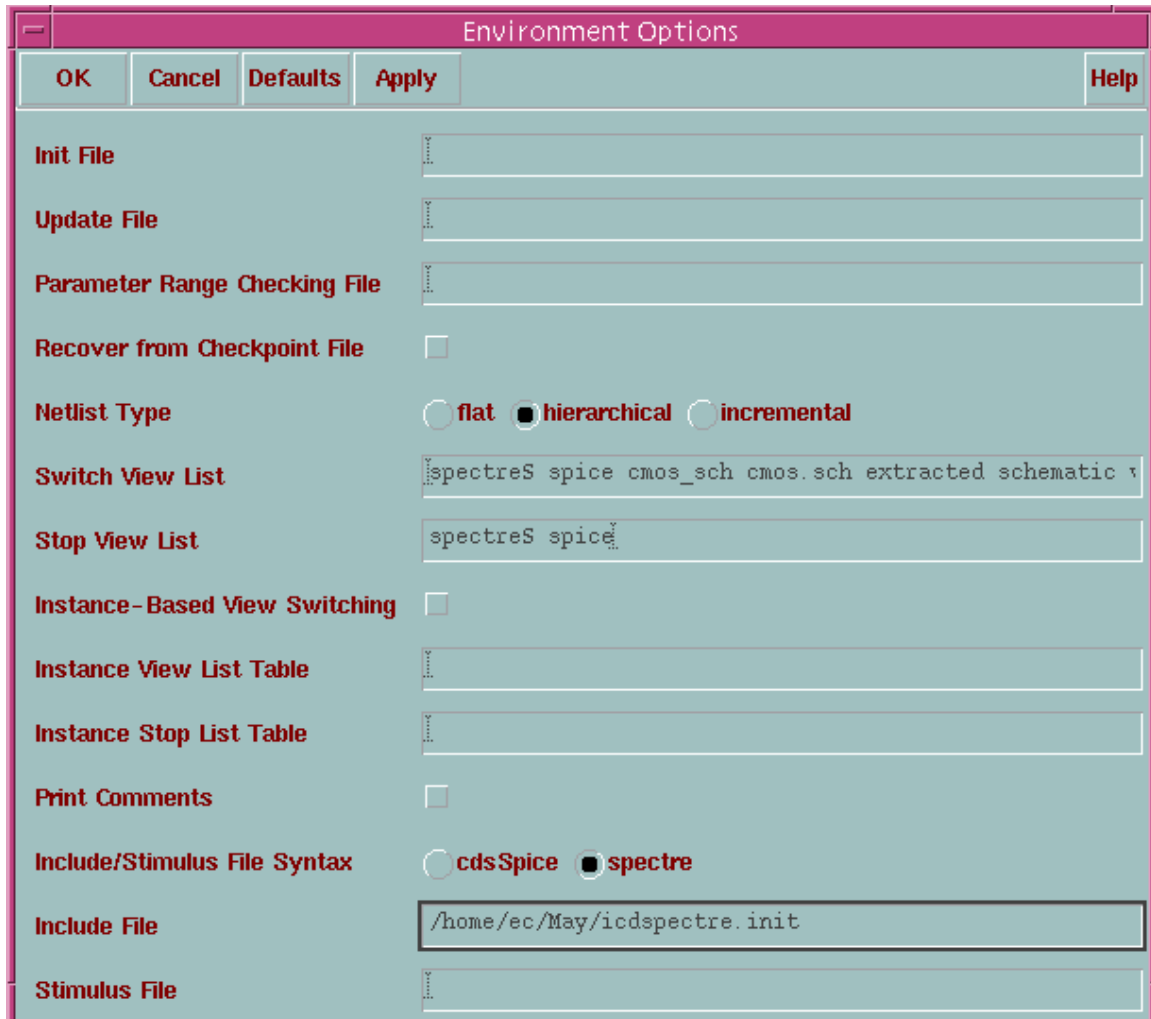
After the LVS run successfully, (it should take some time according to the size of the circuit), you can click the “ *Output* ” to see the detailed report of the comparing and then correct the layout based on it.

Post-simulation

Post-layout simulation is the final verification of the design in software simulation level. It uses the “*extracted*” view to simulate, which is obtained from the extraction of the layout. To use the post-simulation, it is almost the same as what is done in simulation with schematic. We use “*SpectreS*” to do simulation in this example, thus the first is to select the right simulator by menu command in artist window of your test schematic: *Setup / Simulator / Directory / Host...*, and choose the simulator to be “*SpectreS*”.



And then, in the *Setup / Environment* window, add the text “*extracted*” before “schematic”, thus the simulator will use extracted view in priority to do the simulation. The include file “*idcspectre.init*” is to add the *spectreS* MOSFET models. This line should be revised based on the setup directory of your Cadence environment.



Desired result of the post-layout simulation should be very like that in schematic simulation. However, there normally will be some difference because of the parasitic parameters introduced by the layout. If it's acceptable, we can go on to use this layout to fabricate, otherwise we should modify the layout or the design parameters to find out a acceptable solution.

Recommended useful Links,

<http://www.utdallas.edu/~linxf/cadence.html>

<http://www.utdallas.edu/~grinnell>

<http://vlsi.wpi.edu/cds/>