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PROFILE SUMMARY:

- 4.5 years of experience in design and development of video/image processing algorithms, and video codecs and optimization on ARM9/11, TI-DSP (C64x), Intel WMMX (PXA27x/28x) processors for PDA & mobile embedded platforms (WinCE, Symbian, Linux, etc).
- Excellent experience in development of Video Encoders (H.264, MPEG-4 SP & H.263+), Video Decoders (Flash: On2-VP6, Sorensen), Image Codec (JPEG, MJPEG, & PNG).
- Design and development of Motion Estimation, Compensation, Rate Control, CAVLC, CABAC for video codecs, Noise Reduction, De Blur, Video Stabilization, and other Image processing algorithms.
- 2 years of experience in Research and Development in Speech/Audio Signal Processing Algorithms for cochlear implants, speech recognition algorithms.
- In depth knowledge of signal, image, speech processing, and random process concepts
- Well versed with various RISC, SIMD and DSP architectures, and their memory management & programming at assembly level, porting for PDAs/mobiles, and also have experience in FPGA programming of algorithms for Xilinx devices.
- Good knowledge of video security, consumer electronics, video streaming and telephony applications and protocols like (3G-324M), mobile TV (DVB-H).
- Working knowledge on Symbian OS, MS-Mobile OS (WinCE), and Embedded Linux OS and related tools; excellent debugging skills, good experience of project development cycle, CMMi (Level4) process, customer interactions and delivery managements.
- Extensive experience in project development and customer interaction; strong team leading experience, technical presentation and teaching skills.

SKILLS SUMMARY:

Programming Languages: C, C++, Matlab, Assembly Languages of all ARM cores, Intel WMMX Cores, TI DSPs, PERL, VHDL, Verilog.

Embedded Tools: ARM ADS, RVDS, TI CCS, Intel SDT, WinCE, MS Visual Studio, Labview, video stream/quality analysis tools, Rational Purify tools, WinCVS, iPlan, Xilinx.

RTOS/Compilers: WinCE Platform builder, Symbian, Linux- GCC, ARM, & Intel MMX

Architectures: (RISC/SIMD) ARM7x, ARM9x, ARM11, Neon, Intel Xscale, Bulverde, Monhans. (DSPs) C64x, OMAP2430.

EDUCATION:

- **M.S. EE (DSP & Comm)**, University of Texas at Dallas, Dec 2009. GPA: 3.77/4.00.
- **Bachelor of Technology in Electronics & Communication Engg**, National Institute of Technology (NIT), Warangal, India; April 2003, with honors (agg.78.5%, **Class Topper**).
- **Diploma in Electronics & Comm Engg**, 1999, with honors (88.88% - **College Topper**)

ACADEMIC ACHIEVEMENTS

- Class Topper throughout the academic career.
- Secured 34th rank in state level entrance test for Engineering (ECET), 1999, among 25,000

CURRENT POSITION:

Research Assistant, Dept of EE, University of Texas at Dallas (Jan'08 - till date)

- Working for PDA project for Cochlear Implants in Speech Processing Lab.
- Involved in design of **speech processing algorithms** and their optimization on PDAs, and **FPGA programming** for PDA- Cochlear Implant interface board.

PAST WORK EXPERIENCE:

1. Technical Leader, Aricent Pvt. Ltd., Bangalore, India (June 2003 to Dec 2007)

- Design and development of efficient standard video codecs, Image Processing algorithms and optimization on RISC(ARM9x)/SIMD(ARM11/Intel MMX)/DSPs

- Led technical mentoring and project management for a team of size 5-8 members in execution of various customer and in-house projects and interacted with several customers in software requirements design & technical support in day to day work.
- Involved in end-to-end project development life cycles from R&D to product integration for several Image processing and Video Codecs based products
- Part of Technology focus steering committee in initiating and shaping the various road-map projects

PUBLICATIONS

1. Nageswara Rao G, PSSBK Gupta, “Improved Intra Prediction with Multiple Slice Groups for Efficient Packetization in H.264”, IEEE International Conference on Multimedia and Expo (ICME), July 02-05, 2007, Beijing, China.
2. Nageswara Rao G, PSSBK Gupta, “Temporal Motion Prediction for Fast Motion Estimation in Multiple Reference Frames”, IEEE International Symposium on Signal Processing and Information Technology (ISSPIT), August, 2006, Vancouver, Canada.
3. Nageswara Rao G, Prasad RSV, D Jaya Chandra and Srividya Narayanan, “Real-Time Software Implementation of H.264 Baseline Profile Video Encoder for Mobile and Handheld Devices”, ICASSP, May14-19, 2006, Toulouse, France.
4. “Munish Jindal, Nageswara Rao G, “Adaptive block sub-sampling algorithm for motion-estimation on SIMD processors”. The IEEE International Conference on Image Processing (ICIP) Singapore, October 24-27, 2004
5. Krishna A.G, MV Rama Krishna, Nageswara Rao G and PSSBK Gupta, “A Novel Statistical Method for Rate Control in JPEG Encoder”, AVISKAR, organization wide conference, Jan, 2007, Delhi, India, Won First runner-up prize.
6. Nageswara Rao G, D.Jayachandra, N.Rajashekar “An Efficient Digital Sliding controller for Voltage Regulation”, TROYIKA, National Conference at Delhi College of engineering, New Delhi, December, 2002.

PATENTS:

1. Nageswara Rao G, Prasad RSV, Ramkishor K, “**Fixed Rate JPEG Encoding**”, published on Dec 04, 2008 @ US Patent office (USPTO).
2. Jayachandra D, Nageswara Rao G, Prasad RSV, Ramkishor K, Raturaj A Chandpur, “**Method & System for Intelligent and Efficient Camera Motion Estimation for Video Stabilization**”, Published on Sept 24, 2009 @ US Patent office (USPTO).

ACADEMIC WORK:

- **MS Thesis:** Adaptive Psychoacoustic Experiments using PDA research platform cochlear implants, 2009.
- Speech Enhancement and Recognition in Reverberant Environments
- OFMD Equalization design in Doppler channels for Video Telephony Applications

PROJECTS SUMMARY

Following are the list of projects, where I was directly involved in design, implementation, optimization, and testing in one or two member teams. I have also involved indirectly in design discussion and code reviewing tasks of several other image processing projects not mentioned here.

Motion Estimation Algorithms Development for H.264 and MPEG-4 Standards

- Development of Spatio-Temporal Motion Predictor based Motion Estimation algorithm
- Design of Motion Predictors and Early Exit approaches for fast search of motion vectors
- Design of fast Motion estimation till the Quarter pixel accuracy
- Simple Sub-pixel interpolation filters design & memory flow optimization (work is published in ICASSP’ 06)
- Simple & Fast ME for multiple reference frames in H.264 Encoder (published in ISCAS 06)
- Customizing ME Algorithms for various standards (H.264, MPEG-4, H.263+) at different power quality tradeoffs.

Fast and Efficient Intra Prediction Algorithms in H.264

- Designing separate fast Intra prediction mode estimation for I and P frames
- R-D optimization techniques are developed to achieve best quality
- Early exit approaches developed using Spatial directional data and Motion Data (Work is published in ICASSP 06)

Design and Implementation of CAVLC Module for H.264 Encoder

- Implementation of H.264 BP Syntax elements coding (CAVLC) & optimizing the data flow
- Memory-Complexity tradeoffs for coding MB syntax elements and Run Levels
- Estimation of Number of Bits for MB syntax elements and run-levels to perform R-D optimization at various levels

Design, Implementations of MC, Transform, Quant, Recon Modules

- Implementation of prediction filters for estimation of Half-pel, Q-pel block interpolation
- Design of Motion Compensation at integer & sub-pel level, and re-use of computations among ME, MC and Reconstructions
- Design of algorithms to predict zero and fewer coefficients quantized DCT blocks to minimize DCT/IDCT computations.
- Implementation of computationally efficient 2D-DCT (IDCT) and quantization modules

Algorithm Optimization of H.264 BP, MPEG-4 and H.263+ Software Video Encoders for RISC/SIMD processors (ARM9T/9E/11, Xscale,PXA27x/28x)

- Developed various fast techniques for computationally intensive modules of standard video encoder's for low bit rate and limited resource applications
- Design of data flow between different modules in H.264, MPEG-4, H.263+ encoders.
- Complete H.264 BP, MPEG-4 and H.263+ Video encoder components are optimized for various RISC/SIMD/DSP (ARM9T/9E/11, Xscale,PXA27x/28x, etc) architectures.
- Achieved real-time performance on various mobile platforms for different applications

Efficient Error Resilient tools in Video Encoder -Video Conference/Telephony

- Design of Motion Adaptive Intra Refresh (MAIR), Cyclic Intra refresh (CIR) methods
- Estimate Motion Adaptive Packet Sizes (MAPS) for error robustness in encoded stream
- Design of Fast Updates features (Intra Packets, frames updates) for 3G-324M protocol based video telephony applications
- Development of new prediction method with Slice Groups in H.264 to improve the compression with error-resilience (work is published in ICME'07)

Rate Control Algorithm for Standard Video Encoders

- Design of frame level Rate Control for MPEG-4/H.264 Encoders (for RISC/SIMD targets)
 - Deriving the Rate distortion model
 - Bit Budget Estimation for each frame, slices and rate control at slice, frame level
- Design of MB level Rate Control for MPEG-4/H.264 Encoders (for DSP's targets)
 - Bit Budget Estimation for each coded frame
 - Adoption and implementation of TM-5 rate control

In-Loop & out-Loop Filter Development

- Standard in-loop filter implementations in H.263+, H.264 video encoders
- Developed efficient and fast post processing (Out-loop) filters
- Optimization of loop filters on DSPs/ARM platforms

Software Video Stabilization: IP Algorithms Development

- Global Frame Motion Estimation of video sequences captured on hand-held cameras
- Estimate unwanted Camera Motion (Jitter) out of the global motion
- Algorithms design for Camera Motion Correction to remove the motion jitter
- Various algorithms are developed and implemented (worked is filed as a patent)
- Optimized on ARM/DSPs and deployed on video recorders applications

Fixed Rate Control for JPEG

- Fixed Rate JPEG project is initiated by customer interest for applications where it required to ensure no of images in a memory device, image fit into available buffers, and where re-encoding JPEG Images needed by network bandwidth
- Design of Image Adaptive Quantization Table
- Devised a new Rate-Quant (R-Q) model for JPEG (Patent Filed)
- Methods to control file size without quality sacrifice

Flash Video Decoders Optimization on RISC/SIMD (ARM9E, ARM11)

- Sorensen Spark Video Decoder
 - Optimization of Transform, VLD, and Prediction modules on ARM9E and ARM11
- On2's VP6 Video Decoder Optimization
 - Design of data flow to minimize redundant computation and memory access
 - Optimization of Transform, VLD, Prediction and In-Loop filter modules on ARM9E and ARM11 platforms

Motion Detection for Video Surveillance Applications

- Robust Frame and Object Motion Estimation in various Illumination and Noisy conditions
- Design of Motion Detection Solutions for Video Surveillance applications
- Optimization of the algorithms on TI DSP (C64x)

Video Encoders for Video Telephony Applications

- Stringent Rate Control demanded 3G channels developed for Video Telephony applications
- Fine tuning the R-D models and Rate controllers to meet the requirements and minimize quality loss, and buffer latency, etc
- Implemented good error-resilient and concealment schemes
- Video codecs Integrated and tested Video Telephony solution at customer (a top mobile ODM) premises

Image Codecs Implementation on RISC/SIMD/DSPs (ARM9T,9E,11, PXA27xx, TI C64x)

- JPEG/PNG encoders and Decoders implementation on RISC/SIMD/DSPs
- Customized JPEG library creation for Symbian
- Implementation & integration of JPEG codec on highly memory and power limited platforms for Top Chip vendor
- On-Demand transform domain Image operations (Scaling, rotation, overlay, etc) on Symbian and WinCE platforms

Speech Processing Algorithms Design

- LPC, Pitch, Formants Estimation for Speech Signal
- Processing Speech data for Cochlear Implants
- Speech Enhancement against various noisy sources: Weiner, LMS, MMSE filters design
- De-Reverberation of Speech Signal
 - Room Impulse response estimations and Inverse Filter design

Image Pre/Post Processing Algorithms

- Design and development of Adaptive De-Interlace Techniques
- Design of Image Processing solutions for
 - Pre/post processing for Noise suppression, Scaling, Rotation, Mirroring, Color transformations, Video Frame Rate conversions

Milestones in Work at Aricent (Emuzed):

- Achieved best performance for H.264/MPEG-4 encoders on ARM processors among contemporary competitors and won various business deals from top mobile vendors
- Fastest execution of porting and optimization H.264 encoder on ARM-WINCE platforms by single individual (3 months)
- Won cash prizes two times for best papers (Statistical Approach for Fixed rate Image and Rate Control for Video telephony application) at inter-business units at Aricent
- Published 5 conference papers and filed two patents for the work in Aricent/Emuzed