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Matching Analysis and the Design of Low Offset Amplifiers

by

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1 Differential Amp

An important aspect of performance of the N channel source-coupled pair is its input-referred offset voltage. For simplicity assume a MOS differential pair with resistive loads as shown in Figure 1. The differential input voltage

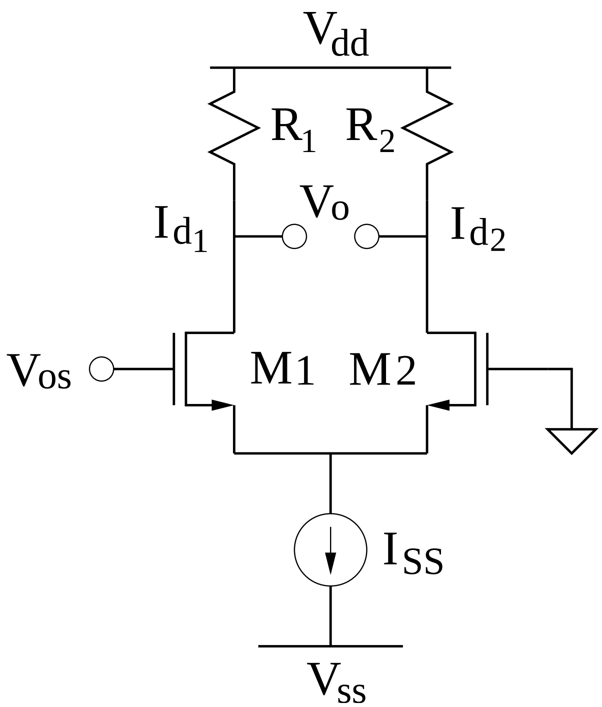

Figure 1: NMOS differential pair with resistor loads

required to force the differential output voltage to zero is the definition of input referred offset voltage, V_{os}. This offset voltage is caused by the fact that the components used to make up the amplifier are not perfectly identical. There are random errors in trying to manufacture two transistors or two resistors that are suppose to be exactly the same. For this simple case we assume that the important mismatches that cause input offset are in the load resistors, the transistor W/L ratio, and the transistor threshold voltage.

Assuming that the two devices are in saturation and neglecting output resistance and body effect, the first order drain current can be written as:

$$I_d = (1/2)\,\mu_n\,C_{ox}\,W/L\;(V_{gs} - V_t)^2\;. \tag{1}$$

Solving equation (1) for V_{gst} yields:

$$V_{gst} \equiv V_{gs} - V_t = \sqrt{\frac{2\,I_d}{\mu_n\,C_{ox}\,W/L}} = \frac{2\,I_d}{g_m}\;, \tag{2}$$

because $g_m = \sqrt{2\,\mu_n\,C_{ox}\,(W/L)I_d}$. Since the input referred offset voltage is the difference in the gate-to-source voltages of the two input transistors, mathematically we can write down the following equation as a definition

$$V_{os} \equiv V_{gs1} - V_{gs2} = \left(V_{t_1} + \frac{2\,I_{d_1}}{g_{m_1}}\right) - \left(V_{t_2} + \frac{2\,I_{d_2}}{g_{m_2}}\right)\;. \tag{3}$$

To proceed with this simple analysis, we need to define some incremental quantities, that is the difference and the average. The general equations are

$$\Delta X = X_1 - X_2 \tag{4}$$

$$X = \frac{X_1 + X_2}{2}\;. \tag{5}$$

Solving for each individual quantity in terms of the difference and average yields

$$X_1 = X + \frac{\Delta X}{2} \tag{6}$$

$$X_2 = X - \frac{\Delta X}{2}\;. \tag{7}$$

Applying this analysis to the offset expression from equation (3), with the appropriate substitutions from equations (6) and (7) gives

$$V_{os} = \left[V_t + \frac{\Delta\,V_t}{2} + \frac{2(I + \Delta I/2)}{g_m + \Delta\,g_m/2}\right] - \left[V_t - \frac{\Delta\,V_t}{2} + \frac{2(I - \Delta I/2)}{g_m - \Delta\,g_m/2}\right]\;. \tag{8}$$

$$V_{os} = \Delta\,V_t + \frac{2\,I}{g_m}\left(\frac{1 + \frac{\Delta I}{2I}}{1 + \frac{\Delta g_m}{2g_m}}\right) - \frac{2\,I}{g_m}\left(\frac{1 - \frac{\Delta I}{2I}}{1 - \frac{\Delta g_m}{2g_m}}\right) \tag{9}$$

Remember that for small $x \ll 1$, the truncated Binomial expansions are as follows: $(1+x)^{-1} \simeq 1-x$ and $(1-x)^{-1} \simeq 1+x$. We will consider that the ΔV_t , ΔI and Δg_m are small enough to apply the truncated Binomial series expansions to equation (9).

$$V_{os} = \Delta V_t + \frac{2I}{g_m} \left[\left(1 + \frac{\Delta I}{2I}\right) \left(1 - \frac{\Delta g_m}{2g_m}\right) - \left(1 - \frac{\Delta I}{2I}\right) \left(1 + \frac{\Delta g_m}{2g_m}\right) \right] . \tag{10}$$

After multiplication of the products in the square braces and canceling terms, the following expression is found.

$$V_{os} = \Delta V_t + \frac{2I}{g_m} \left(\frac{\Delta I}{I} - \frac{\Delta g_m}{g_m} \right) . \tag{11}$$

Next we need to evaluate the terms in the parenthesis. First we will look at the current error term. Since the R's represent an effective *linear* resistor, we can write a KVL loop for the condition when the differential output voltage is zero.

$$I_1 R_1 = I_2 R_2 , \qquad \text{when} \quad \Delta V_o = 0 . \tag{12}$$

Again we use incremental quantities to analyze equation (12).

$$(I + \Delta I/2)(R + \Delta R/2) = (I - \Delta I/2)(R - \Delta R/2) . \tag{13}$$

$$IR \left(1 + \frac{\Delta I}{2I}\right) \left(1 + \frac{\Delta R}{2R}\right) = IR \left(1 - \frac{\Delta I}{2I}\right) \left(1 - \frac{\Delta R}{2R}\right) . \tag{14}$$

Therefore by inspection of equation (14) we see that

$$\frac{\Delta I}{I} = -\frac{\Delta R}{R} \tag{15}$$

For the second term in equation (11), we write the equations for the transconductance of both of the input transistors as: $g_{m_1} = \sqrt{2\mu_n C_{ox} S_1 I_1}$ and $g_{m_2} = \sqrt{2\mu_n C_{ox} S_2 I_2}$. Let $S \equiv W/L$ to simplify the algebra. Again we apply the incremental quantity analysis on the transconductance, therefore we start with

$$\begin{aligned}\Delta g_m = g_{m_1} - g_{m_2} = & \sqrt{2\,\mu_n\,C_{ox}\,(S+\Delta S/2)(I+\Delta I/2)} \\ & -\sqrt{2\,\mu_n\,C_{ox}\,(S-\Delta S/2)(I-\Delta I/2)}\,. \end{aligned} \tag{16}$$

To proceed we need to linearize equation (16) by applying the Binomial series expansion and truncating it to only include terms of first order. That is: $\sqrt{1 \pm x} \approx 1 \pm x/2$, for small x. Making this substitution and some algebraic manipulation yields

$$\frac{\Delta g_m}{g_m} = \left(1 + \frac{\Delta S}{4S} + \frac{\Delta I}{4I}\right) - \left(1 - \frac{\Delta S}{4S} - \frac{\Delta I}{4I}\right)\,. \tag{17}$$

$$\frac{\Delta g_m}{g_m} = \frac{\Delta S}{2S} + \frac{\Delta I}{2I}\,. \tag{18}$$

We can substitute equation (18) back into the V_{os} equation (11) to get

$$V_{os} = \Delta\,V_t + \frac{2\,I}{g_m}\left[\frac{\Delta I}{I} - \left(\frac{\Delta S}{2S} + \frac{\Delta I}{2I}\right)\right]\,. \tag{19}$$

$$V_{os} = \Delta\,V_t + \frac{2\,I}{g_m}\left(\frac{\Delta I}{2I} - \frac{\Delta S}{2S}\right)\,. \tag{20}$$

Finally substitute equation (15) into equation (20)

$$V_{os} = \Delta\,V_t + \frac{2\,I}{g_m}\left(-\frac{\Delta R}{2R} - \frac{\Delta S}{2S}\right)\,. \tag{21}$$

$$V_{os} = \Delta\,V_t - \frac{I}{g_m}\left(\frac{\Delta R}{R} + \frac{\Delta S}{S}\right)\,. \tag{22}$$

The minus sign in equation (22) is not really meaningful because ΔR and ΔS can both be either positive or negative by the way that we defined them. By studying equation (22), note that the input offset voltage is a direct function of the threshold voltage mismatch, which results in a constant offset that is bias point independent. Threshold mismatch is a strong function of the process uniformity and area of the device. By using a common-centroid layout and large area devices, a substantial improvement can be made in in this mismatch.

Next notice that for a given percentage mismatch in the load elements and/or the input devices W/L ratio, the input offset scales directly with the bias dependent factor I/g_m. For MOSFETs this factor is equal to $(V_{gs}-V_t)/2$. Clearly to make the load and the input device W/L ratio mismatches minimal we need to bias the input differential pair with a low V_{gst}. You can not make V_{gst} arbitrarily small since this will force the input transistors into subthreshold conduction. This condition happens at approximately 78 mV at room temperature. Once in subthreshold you will not gain any more improvement in reducing the offset.

2 Current Mirrors

Another important building block that analog circuit designers need to understand the effect of transistor mismatches to its performance is the MOS current mirror or current source. These could be used as active loads in amplifiers or as an accurate bias for an amplifier. Also they are an integral part of current steering DACs. In order to analyze this problem consider the circuit diagram of two N-channel MOSFETs shown in Figure 2 below. Note that this circuit forces both devices to have the same V_{DS}. If the two transistors had different drain-to-source voltages the output conductance, due to channel length modulation, would have to be accounted for. We are only interested in the effect of device mismatch between two identical devices biased at exactly the same condition.

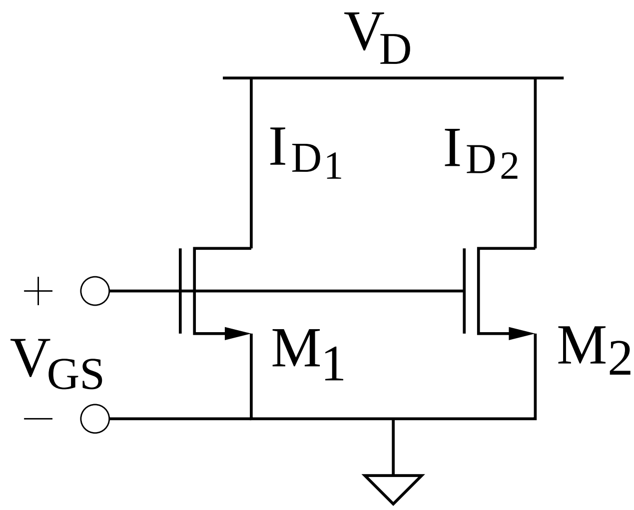

Figure 2: Matched pair of MOS current sources

We will assume the important mismatches are due to threshold voltage and W/L ratio. Using the first order MOS model we can write the drain currents for M1 and M2 noting that they have the same gate-to-source voltage and assuming that they are always in saturation, therefore:

$$I_{D_1} = (1/2)\,\mu_n C_{ox}\,(W/L)_1\,\left(V_{GS} - V_{t_1}\right)^2 \;, \tag{23}$$

$$I_{D_2} = (1/2)\,\mu_n C_{ox}\,(W/L)_2\,\left(V_{GS} - V_{t_2}\right)^2 \;. \tag{24}$$

Let $S \equiv W/L$ and define average and difference quantities as:

$$\Delta I_D = I_{D_1} - I_{D_2} \qquad I_{D_1} = I_D + \frac{\Delta I_D}{2} \tag{25}$$

$$I_D = \frac{I_{D_1} + I_{D_2}}{2} \qquad I_{D_2} = I_D - \frac{\Delta I_D}{2} \tag{26}$$

$$\Delta V_t = V_{t_1} - V_{t_2} \qquad V_{t_1} = V_t + \frac{\Delta V_t}{2} \tag{27}$$

$$V_t = \frac{V_{t_1} - V_{t_2}}{2} \qquad V_{t_2} = V_t - \frac{\Delta V_t}{2} \tag{28}$$

$$\Delta S = S_1 - S_2 \qquad S_1 = S + \frac{\Delta S}{2} \tag{29}$$

$$S = \frac{S_1 - S_2}{2} \qquad S_2 = S - \frac{\Delta S}{2} \tag{30}$$

We start by subtracting equation (24) from (23) which yields

$$\Delta I_D = I_{D_1} - I_{D_2} = \frac{1}{2}\,\mu_n\,C_{ox}\left[S_1\,(V_{GS} - V_{t_1})^2 - S_2\,(V_{GS} - V_{t_2})^2\right]\;. \qquad (31)$$

Substituting for the average and difference equations from above yields:

$$\Delta I_D = \frac{1}{2}\,\mu_n\,C_{ox}\left\{\left(S + \frac{\Delta S}{2}\right)\left[V_{GS} - \left(V_t + \frac{\Delta V_t}{2}\right)\right]^2 - \left(S - \frac{\Delta S}{2}\right)\left[V_{GS} - \left(V_t - \frac{\Delta V_t}{2}\right)\right]^2\right\} \qquad (32)$$

$$\Delta I_D = \frac{1}{2}\,\mu_n\,C_{ox}\,S\left\{\left(1 + \frac{\Delta S}{2S}\right)\left[V_{GS} - V_t - \frac{\Delta V_t}{2}\right]^2 - \left(1 - \frac{\Delta S}{2S}\right)\left[V_{GS} - V_t + \frac{\Delta V_t}{2}\right]^2\right\} \qquad (33)$$

$$\Delta I_D = \frac{1}{2}\,\mu_n\,C_{ox}\,S\left\{\left(1 + \frac{\Delta S}{2S}\right)\left[(V_{GS} - V_t)^2 - (V_{GS} - V_t)\Delta V_t + \left(\frac{\Delta V_t}{2}\right)^2\right] - \left(1 - \frac{\Delta S}{2S}\right)\left[(V_{GS} - V_t)^2 + (V_{GS} - V_t)\Delta V_t + \left(\frac{\Delta V_t}{2}\right)^2\right]\right\} \qquad (34)$$

$$\Delta I_D = \frac{1}{2}\,\mu_n\,C_{ox}\,S\left\{\frac{\Delta S}{S}\left[(V_{GS} - V_t)^2 + \Delta V_t^2/4\right] - 2\,(V_{GS} - V_t)\,\Delta V_t\right\}. \qquad (35)$$

Since the difference quantities must be small in order for this analysis to be valid, then the higher-order terms of these deltas should be negligibly small. Therefore we drop that term and get,

$$\Delta I_D = \underbrace{\frac{1}{2}\,\mu_n\,C_{ox}\,S\,(V_{GS} - V_t)^2}_{I_D}\left[\frac{\Delta S}{S} - \frac{2\,\Delta V_t}{V_{GS} - V_t}\right]\;. \qquad (36)$$

So the fractional mismatch can be written as

$$\frac{\Delta I_D}{I_D} = \frac{\Delta(W/L)}{(W/L)} - \frac{2\,\Delta V_t}{V_{GS} - V_t}\ . \tag{37}$$

Remember the minus sign does not mean that these two terms cancel each other. Because the difference terms can have either sign they can be additive or subtractive. Equation (37) shows that the first component of the current mismatch is geometry dependent but independent of the bias point. The second term is due to the threshold voltage mismatch and increases as the value of V_{GST} is reduced. This occurs because the fixed threshold voltage mismatch progressively becomes a larger fraction of the total gate drive that is applied to the two transistors and therefore contributes a progressively larger percentage error as V_{GST} becomes small. The practical significance of this fact is that because the threshold voltage can have a considerable gradient across a chip, care must be taken in biasing current sources from the same voltage bias connection when the devices are physically separated by large distances. Large percentage errors ($>$ 10 %) can result in the current between devices which are widely separated and operated at very small values of V_{GST}. This means that you should distribute the bias around a chip by routing currents to local current mirrors. Also, note that by segmenting the current source transistors into multiple units and laying them out using either a common centroid or inter-digitation geometry will reduce the current mismatch due to the second term if the ΔV_t is caused by a linear gradient in the threshold adjust implant.

The type of analysis shown in the previous two sections demonstrate the general ideas of how to improve mismatch in a differential pair or simple current mirror. It gave us some insight into the problem, but this style of analyzing offset using incremental quantities for complete opamps would be very tedious. Also, we don't have a model relating the incremental values to actual MOSFETs in a particular process. So we can not make a calculation of the offset. We need an improved type of analysis. Considering mismatch a stochastic process and assigning random variables to do the analysis is the way forward. Statistics on devices in a given CMOS process can be measured, including mismatch, and used to find models that can be employed to calculate standard deviations of offset for a particular amplifier. This can be done by hand or in a computer program such as SPICE. This general method is often called the Pelgrom model.

3 Pelgrom Model for Transistor Matching

The difference between two identical devices on the same chip that is created by the manufacturing process is called *mismatch*. The processing causes time-independent random variations in some physical quantities of identical transistors. Therefore we can describe statistically the outcomes for many processing runs through the fab. The measurements from each matched pair of devices on all wafers in multiple fabrication runs make up a large ensemble. With this large dataset, models can be made for the variance of certain physical properties of identical transistors. These variances do not change in time, but are constant once the devices are manufactured. The variation comes from the inability of the manufacturing line to produce the exact same device characteristics, both in physical dimension and in electrical function, for side-by-side transistors on any given process lot.

A model was developed by Pelgrom et. al. by studying mismatch between rectangular devices of equal area using Fourier analysis on the frequency components produced by spatial (not temporal) differences. They found that the variance (σ^2) of parameter ΔP is given by

$$\sigma^2(\Delta P) = \frac{\mathcal{A}_{P}^2}{WL} + S_{P}^2\, D_x^2\ , \tag{38}$$

where $\mathcal{A}_P$ is the area proportionality constant for parameter P, S_P describes the variation with the spacing and D_x is the distance between devices in the x direction. The second term in equation (38) is important for matching in DACs, but in amplifier design it is not considered because the critical devices to offset are always layed-out next to each other. So we will ignore this term.

To apply this type of model to a MOSFET, we start with the $I-V$ equation and note what can vary with manufacture of the device. The parameters are: width, length, mobility, gate oxide thickness, and threshold voltage. We can apply equation (38) without the spacing term to write the variance of parameter V_{t0} as

$$\sigma^2(V_{t0}) = \frac{\mathcal{A}_{V_{t0}}^2}{WL} , \tag{39}$$

where the standard deviation of V_{t0} is characterized with the constant $\mathcal{A}_{V_{t0}}$. The zero subscript denotes that this is the fixed part of the threshold voltage (no back-gate bias). This constant is found from a linear regression fit on the data taken on a large number of different area MOSFETs. The remaining parameters make up whats called the current gain factor $\beta = \mu C_{ox} W/L$. The matching properties of β are derived from the fact that the parameters that make up β are mutually independent. So their variances are additive.

$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{\sigma^2(\mu)}{\mu^2} + \frac{\sigma^2(C_{ox})}{C_{ox}^2} + \frac{\sigma^2(W)}{W^2} + \frac{\sigma^2(L)}{L^2} . \tag{40}$$

The mismatch generating processes for the mobility and gate oxide will be modeled using equation (38) without the spacing term. The remaining parameters in the β factor, W and L, have additional terms to be included. These extra variations originate from edge roughness. A one-dimensional Fourier analysis of edge roughness leads to $\sigma^2(W) \propto 1/L$ and $\sigma^2(L) \propto 1/W$. Therefore equation (40) becomes after substitution

$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{\mathcal{A}_{\mu}^2}{WL} + \frac{\mathcal{A}_{C_{ox}}^2}{WL} + \frac{\mathcal{A}_{W}^2}{W^2 L} + \frac{\mathcal{A}_{L}^2}{WL^2} . \tag{41}$$

Equation (41) can be approximated for large enough W and L (which must be determined by measurement for each process) as

$$\frac{\sigma^2(\beta)}{\beta^2} \simeq \frac{\mathcal{A}_{\beta}^2}{WL} , \tag{42}$$

where the effects of all of the process related constants, $\mathcal{A}_{\mu}$, $\mathcal{A}_{C_{ox}}$, $\mathcal{A}_{W}$, and $\mathcal{A}_{L}$ are included in $\mathcal{A}_{\beta}$.

Now with this statistical model we can analyze the variation in the drain current for a fixed gate-to-source voltage. This gives the following

$$\frac{\sigma^2(I_D)}{I_D^2} = \frac{4\,\sigma^2(V_{t0})}{(V_{GS} - V_{t0})^2} + \frac{\sigma^2(\beta)}{\beta^2} . \tag{43}$$

Equation (43) is basically equivalent to equation (37) from the incremental analysis. It should be pointed out that the first term on the right-hand side of equation (43) will not "blow-up" as the device bias in reduced until the transistor goes into subthreshold. It will become independent of gate voltage with a value of $q^2\,\sigma^2(V_{t0})/(nkT)^2$. We can re-write equation (43) using the first order transconductance relationship

$$\frac{\sigma^2(I_D)}{I_D^2} = \left(\frac{g_m}{I_D}\right)^2 \sigma^2(V_{t0}) + \frac{\sigma^2(\beta)}{\beta^2} \ . \tag{44}$$

The statistical errors associated with mismatch can be considered, from a circuit point of view, as a small signal. We can use the small-signal, linear model of a MOSFET to manipulate equation (44). We can write: $\sigma^2(I_D) = g_m^2\,\sigma^2(V_g)$. Applying this relationship to equation (44) yields

$$\sigma^2(V_g) = \sigma^2(V_{t0}) + \left(\frac{I_D}{g_m}\right)^2 \frac{\sigma^2(\beta)}{\beta^2} \ . \tag{45}$$

For a well designed opamp, the input stage devices are biased such that $I_D/g_m \ll 1$, therefore only the first term in equation (45) is important. Also to make writing the circuit equations easier we will simplify the notation.

$$\sigma_{v_t}^2 \equiv \sigma^2(V_{t0}) = \frac{\mathcal{A}_{V_{t0}}^2}{WL} \equiv \frac{\mathcal{A}_{v_t}^2}{WL} \ . \tag{46}$$

Note that the $\mathcal{A}_{v_t}$'s will be different depending on type of transistor and whether the transistors are cross-coupled, inter-digitated, or side-by-side.

Now we will analyze a basic two stage transconductance amplifier. The analysis proceeds like a noise analysis of this amp. This should not be surprising since we have constructed a stochastic model for the offset.

4 Input Offset of Two-Stage Transconductance Amp

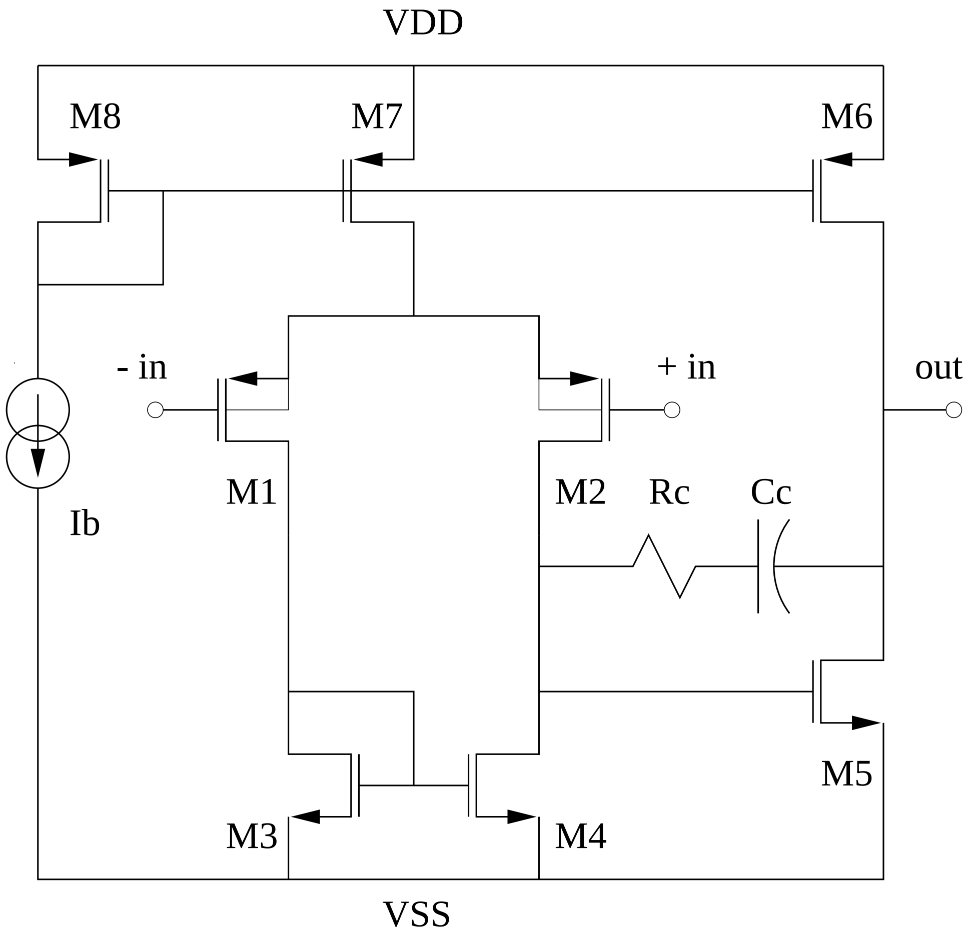

Figure 3: Two stage CMOS transconductance amplifier with PMOS inputs

To begin the offset analysis of the Transconductance (TC) Amp above:

- Only devices in the signal path are important
- Second gain stage (M5 & M6) random offset not important because when referred to the input it's divided by the square of the first stage gain
- M7's mismatch is canceled by symmetry
- Must account for mismatches of (M1 − M4)
- Start by summing currents at drains (M2 & M4)

4.1 General Equation for Two-Stage TC Amp

We start the analysis by writing down the small-signal power equation for the Two-Stage TC amp by summing all the $\overline{i_d^2}$ for transistors M1 − M4. That leads to the following equation

$$\overline{i_o^2} = g_{m_1}^2\sigma_{v_{t1}}^2 + g_{m_2}^2\sigma_{v_{t2}}^2 + g_{m_3}^2\sigma_{v_{t3}}^2 + g_{m_4}^2\sigma_{v_{t4}}^2 \ . \tag{47}$$

Because of symmetry of the differential input pair and load pair, we can reduce equation (47) to

$$\overline{i_o^2} = 2g_{m_2}^2\sigma_{v_{t2}}^2 + 2g_{m_4}^2\sigma_{v_{t4}}^2 \ . \tag{48}$$

Equation (48) gives the total mismatch current power at the output of the first stage, but we want to refer this back to the input of the amp as a unique point so different amplifiers can be compared.

$$\overline{v_{os}^2} = \frac{\overline{i_o^2}}{g_{m_2}^2} = 2\left[\sigma_{v_{t2}}^2 + \left(\frac{g_{m_4}}{g_{m_2}}\right)^2\sigma_{v_{t4}}^2\right] \ . \tag{49}$$

Equation (49) is the general equation for offset in the Two-Stage TC amplifier. It can be used to determine the canonical input-referred offset for any given variance σ_v^2 which has a known physical model. We have such a model in equation (46). Now insert the expression (46) into the general equation (49) for the two stage amp. After applying some algebra we get the variance of the input-referred offset

$$\overline{v_{os}^2} = 2\left[\frac{\mathcal{A}_{v_t,p}^2}{W_2L_2} + \left(\frac{\mu_n S_4}{\mu_p S_2}\right)\frac{\mathcal{A}_{v_t,n}^2}{W_4L_4}\right] \ , \tag{50}$$

where the p and n subscripts denote PMOS and NMOS transistors respectfully. After factoring out the term related to the input transistors we get the following equation for the variance of the input referred offset

$$\overline{v_{os}^2} = 2\,\frac{\mathcal{A}_{v_t,p}^2}{W_2L_2}\left[1 + \frac{\mu_n\mathcal{A}_{v_t,n}^2}{\mu_p\mathcal{A}_{v_t,p}^2}\left(\frac{L_2}{L_4}\right)^2\right] \tag{51}$$

Note the variance of the offset voltage has the same form as the variance of the $1/f$ noise voltage variance for the same two stage amp. When we study equation (51), we see that it is quadratic in L_2, so there is a minimum which can be found by taking a derivative and equating the result to zero. This leads to the following expression.

$$\frac{\partial \overline{v_{os}^2}}{\partial L_2} = 0\,, \longrightarrow \; L_2 = \sqrt{\frac{\mu_p}{\mu_n}}\,\frac{\mathcal{A}_{v_t,p}}{\mathcal{A}_{v_t,n}}\,L_4 \tag{52}$$

Again note how the form of equation (52) is similar to the $1/f$ optimum equation for the input device channel length.

For CMOS processes that employed n-type poly gates, the ratio of the input gate length to the load gate length was always about the same number for mismatch and $1/f$ noise. The PMOS transistors matched better and had a smaller KF parameter. It was speculated that there was some relationship involved. However, there is no physical relationship between mismatch and $1/f$ noise other than they both scale with the inverse of gate area. In newer CMOS processes, with both n-doped and p-doped poly gates, this ratio is not the same number.

4.2 Summary: Input Referred Offset Voltage

- W_2 and L_4 are independent parameters
- So increasing either will decrease input referred offset
- After L_4 is choosen, then L_2 is found by the optimization relation
- It has been suggested that **input offset** can be considered the **limit** of $1/f$ **noise** extrapolated to DC, however this is not physically true
- **But in general good low frequency noise design is also good for offset for processes with n-doped poly gates**

5 Input Offset of Folded-Cascode Amp

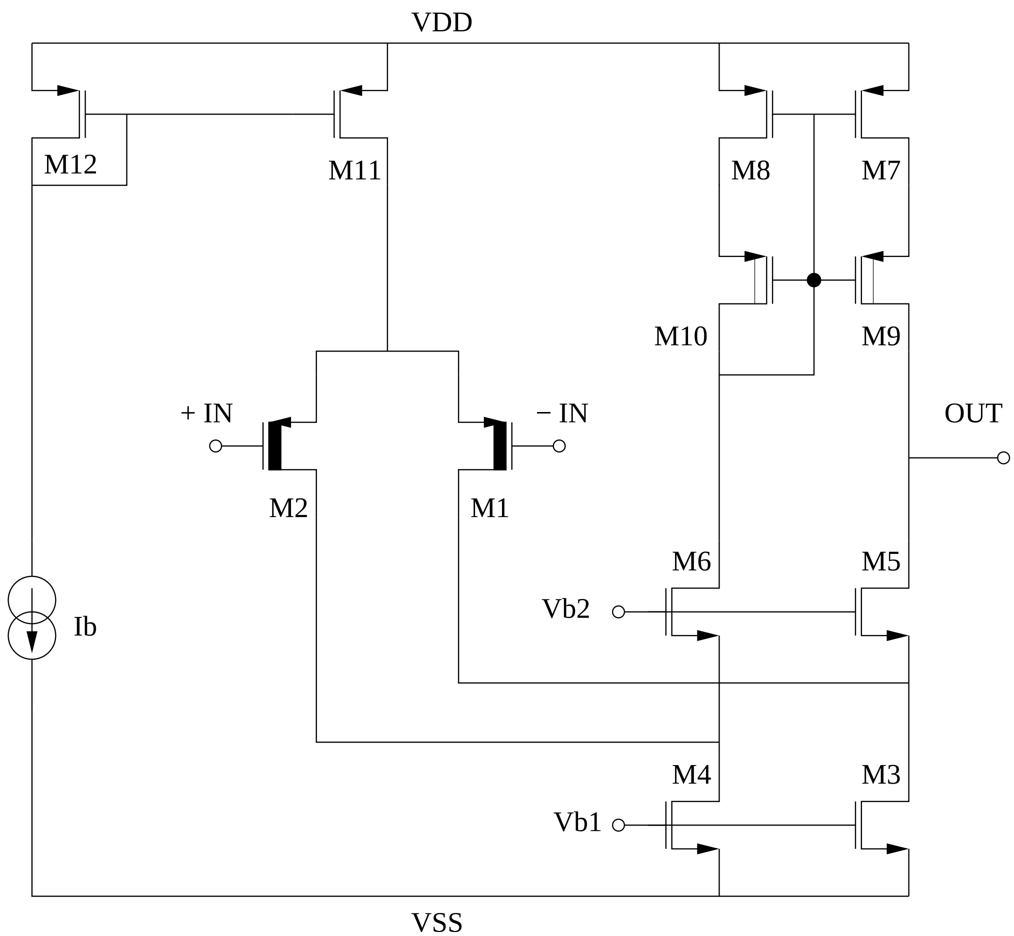

Figure 4: Folded-Cascode amplifier with Depletion PMOS inputs

To begin the offset analysis on the Folded-Cascode TC amp above:

- Only devices in the signal path are important
- M11's mismatch is canceled by symmetry
- Must account for mismatches of (M1 − M10)
- The cascode devices are special cases
- Start by summing currents at the output

5.1 General Analysis of Folded Cascode Amp

The varaince in the total current summed at the output is

$$\begin{aligned}\overline{i_o^2} &= g_{m_1}^2\sigma_{v_{t1}}^2 + g_{m_2}^2\sigma_{v_{t2}}^2 + g_{m_3}^2\sigma_{v_{t3}}^2 + g_{m_4}^2\sigma_{v_{t4}}^2 + G_{m_5}^2\sigma_{v_{t5}}^2 \\ &+ G_{m_6}^2\sigma_{v_{t6}}^2 + g_{m_7}^2\sigma_{v_{t7}}^2 + g_{m_8}^2\sigma_{v_{t8}}^2 + G_{m_9}^2\sigma_{v_{t9}}^2 + G_{m_{10}}^2\sigma_{v_{t10}}^2 \ .\end{aligned} \tag{53}$$

Because of symmetry, the equation becomes

$$\overline{i_o^2} = 2\left(g_{m_1}^2\sigma_{v_{t1}}^2 + g_{m_3}^2\sigma_{v_{t3}}^2 + G_{m_5}^2\sigma_{v_{t5}}^2 + g_{m_7}^2\sigma_{v_{t7}}^2 + G_{m_9}^2\sigma_{v_{t9}}^2\right) \ . \tag{54}$$

$G_m \equiv$ effective transconductance with source degeneration.

$$G_{m_5} = \frac{g_{m_5}}{1 + g_{m_5}\left(r_{d_1} || r_{d_3}\right)}; \qquad G_{m_9} = \frac{g_{m_9}}{1 + g_{m_9} r_{d_7}} \ . \tag{55}$$

Since $g_m r_d > 10^2$ then $G_m^2 \simeq g_m^2/10^4$ therefore we may ignore the cascode devices. Then the output current variance is

$$\overline{i_o^2} = 2\left(g_{m_1}^2\sigma_{v_{t1}}^2 + g_{m_3}^2\sigma_{v_{t3}}^2 + g_{m_7}^2\sigma_{v_{t7}}^2\right) \ . \tag{56}$$

Referring back to the input through the square of the transconductance gives the input offset voltage variance

$$\overline{v_{os}^2} = \frac{\overline{i_o^2}}{g_{m_1}^2} = 2\left[\sigma_{v_{t1}}^2 + \left(\frac{g_{m_3}}{g_{m_1}}\right)^2 \sigma_{v_{t3}}^2 + \left(\frac{g_{m_7}}{g_{m_1}}\right)^2 \sigma_{v_{t7}}^2\right] \ . \tag{57}$$

Substituting the model for $\sigma_{v_t}^2$ and g_m results in an equation for the variance of the input referred offset voltage

$$\overline{v_{os}^2} = 2\,\frac{\mathcal{A}_{v_t,1}^2}{W_1 L_1}\left[1 + 2.7\,\frac{k'_{n425}\mathcal{A}_{v_t,3}^2}{k'_{p800}\mathcal{A}_{v_t,1}^2}\left(\frac{L_1}{L_3}\right)^2 + 1.7\,\frac{k'_{p425}\mathcal{A}_{v_t,7}^2}{k'_{p800}\mathcal{A}_{v_t,1}^2}\left(\frac{L_1}{L_7}\right)^2\right] \ , \tag{58}$$

where $k' = \mu C_{ox}$ for the particular type device. The bias current ratios used in this design are $I_{D3}/I_{D1} = 2.7$, $I_{D7}/I_{D1} = 1.7$. The $\mathcal{A}_{v_t}$'s are found from matching data taken by the fabs. This particular design is in LBC3S. Plots of the V_t matching data for the NMOS and PMOS devices is shown in

Figures 5 & 6. The $\mathcal{A}_{v_t}$ is the slope of the data. The Depletion PMOS plot is not shown. The data for the three types of transistors used in this circuit are: $\mathcal{A}_{v_t,1} = 38.7$ mVμm for the 800 Å Poly 2, cross-coupled, Depletion PMOS; $\mathcal{A}_{v_t,3} = 71.7$ mVμm for the 425 Å Poly 1, cross-coupled, NMOS; and $\mathcal{A}_{v_t,7} = 31.3$ mVμm for the 425 Å Poly 1, interleaved, PMOS. Because this amp employs transistors with different gate oxide thickness, we can not cancel C_{ox} from equation (58). By inspecting equation (58), we see that W_1, L_3 and L_7 are independent parameters. If we increase any one of them, the input-referred offset voltage with decrease. However the input transistor gate length is a dependent parameter and can not be set to any value if low offset is desired. Next we will see how to optimize L_1.

5.2 Optimization of Random Offset Voltage

Because of the resulting $\overline{v_{os}^2}$ expression is a quadratic equation in L_1, there is a minimum which can be found computing the partial derivative $\frac{\partial \overline{v_{os}^2}}{\partial L_1} = 0$. Performing the calculus and after some algebraic manipulation we get

$$\frac{1}{L_1^2} = 2.7\,\frac{k'_{n_{425}}}{k'_{p_{800}}}\left(\frac{\mathcal{A}_{v_t,3}}{\mathcal{A}_{v_t,1}}\right)^2\frac{1}{L_3^2} + 1.7\,\frac{k'_{p_{425}}}{k'_{p_{800}}}\left(\frac{\mathcal{A}_{v_t,7}}{\mathcal{A}_{v_t,1}}\right)^2\frac{1}{L_7^2}\,. \tag{59}$$

The process parameters for the respective NMOS and PMOS transistors in LBC3S are: $k'_{p_{800}} = 12.76\mu\text{A/V}^2$, $k'_{n_{425}} = 21.79\mu\text{A/V}^2$, $k'_{p_{425}} = 6.72\mu\text{A/V}^2$. After choosing $L_3 = 20\mu$m and $L_7 = 32\mu$m to meet other electrical specs, we can substitute these parameters into equation (59) and then calculate an optimum electrical length for the input transistor, $L_1 = 4.81\mu$m. For LBC3S the total lateral diffusion, $TLD = 0.74\mu$m, so we add this to the optimal electrical channel length and get $L_1 = 5.55\mu$m. This value is off the drawing grid, so I will use $L_1 = 6\mu$m.

5.3 Calculation of Random Offset Voltage

For the bias point chosen in this design the $I_D^2/g_m^2 \approx 10^{-3}$, so only the V_t mismatch needed to be considered for calculating the input referred offset voltage. Therefore the error power or variance of the input offset can be calculated with the following equation.

$$\overline{v_{os}^2} = 2\left[\frac{\mathcal{A}_{v_t,1}^2}{W_1 L_1} + \left(\frac{g_{m_3}}{g_{m_1}}\right)^2 \frac{\mathcal{A}_{v_t,3}^2}{W_3 L_3} + \left(\frac{g_{m_7}}{g_{m_1}}\right)^2 \frac{\mathcal{A}_{v_t,3}^2}{W_7 L_7}\right] \tag{60}$$

Substituting the transconductances at the bias point and the electrical values for the W's and L's given the transistor drawn sizes in μm of $S_1 = 400/6$, $S_3 = 96/32$, and $S_3 = 40/20$ gives a variance of $\overline{v_{os}^2} = 6.359 \times 10^{-6}$ so the one sigma input referred offset voltage is $\sigma_{os} = \pm 2.52$ mV. So the worst case, input offset would be $3\,\sigma_{os} = \pm 7.56$ mV.

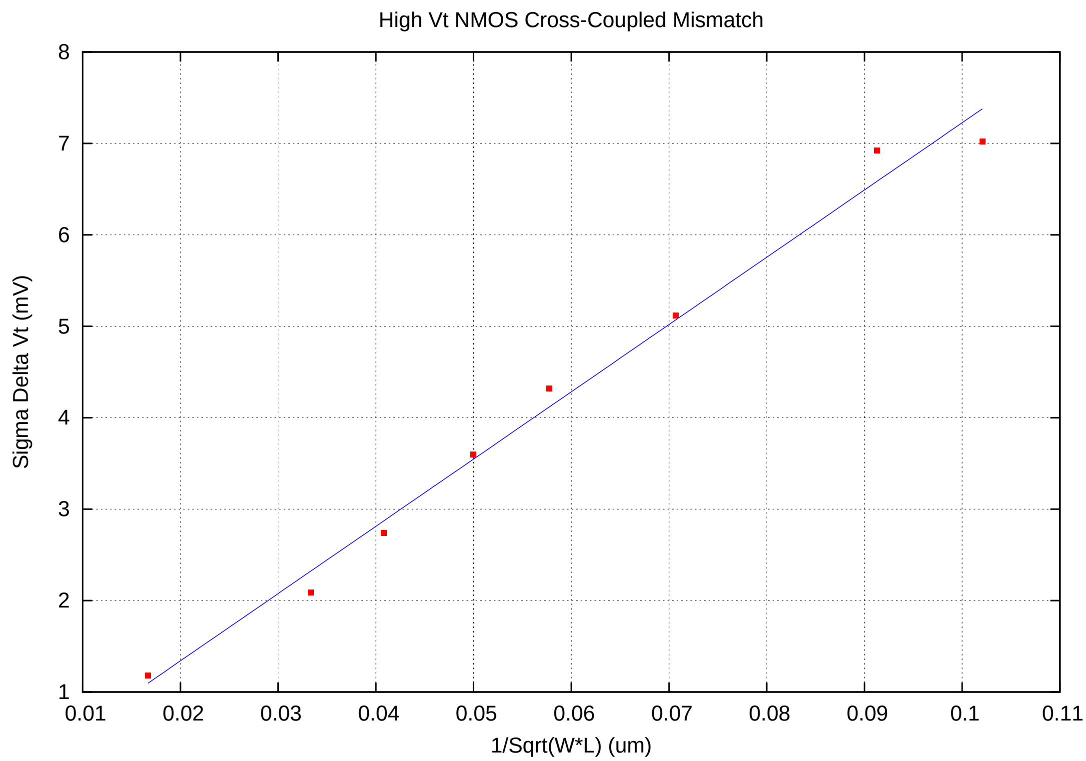

Figure 5: NMOS V_t mismatch; $y = 71.7x$

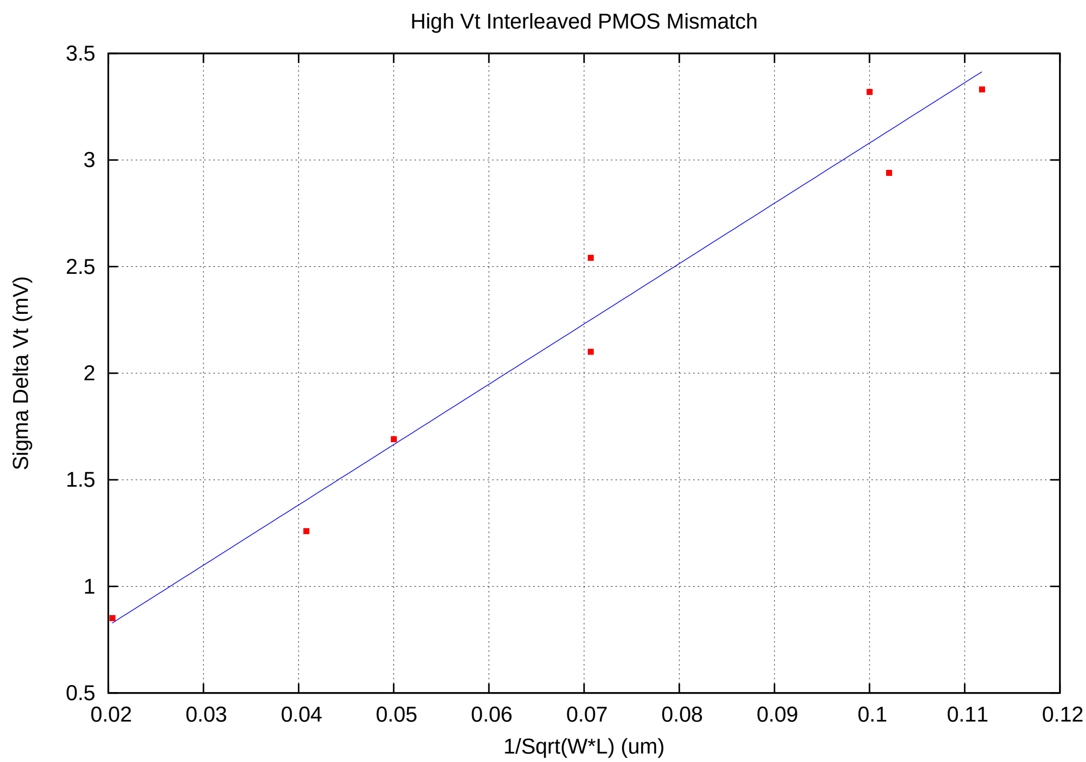

Figure 6: PMOS V_t mismatch; $y = 31.3x$