

**EE7329-501**  
**Homework # 3**

Due: Wednesday, March 1

Download the netlist of the fully-differential op-amp on the web-page. You can not change the netlist. Design the op-amp to meet the following specification:  $A_v \geq 100\text{dB}$ ,  $f_u \geq 16\text{MHz}$ , phase margin  $PM \geq 70^\circ$ , gain margin  $GM \geq 20\text{dB}$ . The noise  $\overline{v_{1/f}^{2\frac{1}{2}}} \leq 915\text{nV}/\sqrt{\text{Hz}} @ 1\text{Hz}$  and  $\overline{v_{thermal}^{2\frac{1}{2}}} \leq 5.2\text{nV}/\sqrt{\text{Hz}} @ 1\text{MHz}$ . The small-signal settling time  $T_{s_{small}} \leq 700\text{ns}$  for a 100mV step to 0.1% of final value (in a closed-loop, inverting gain of 1). The output must swing  $5V_{pp}$  (in a closed-loop, inverting gain of 2) with a 3V supply and achieve a  $THD \leq 1 \times 10^{-4}\%$ .

The bias current  $I_b = 10\mu\text{A}$ . The total current must be less than 1.2 mA not counting  $I_b$ . The load for the amp is  $R_L = 50\text{k}\Omega || C_L = 5\text{pF}$ .

You must use the SPICE input stimulus files given on the web-page for the analysis of your amplifier for OP, AC, NOISE, THD & swing, TRAN (small-signal settling).

Turn in a schematic drawing of your **complete** circuit with all devices labeled as the netlist and give all active and passive device sizes on the schematic or in a Table. Edited SPICE analysis of your circuit for all conditions that prove you met all of the specs (include OP, AC, NOISE, THD, TRAN analysis). Turn in SPICE print files of bias condition and plots of AC Bode analysis, TRAN step response and maximum sine wave time domain simulation and harmonic distortion.