

EE7329-501

Semester Project

Due: Monday, April 23

The semester project is to design and simulate a complete Power Operational Amplifier system that can drive a 32Ω speaker differentially. You can design a fully-differential Op-Amp or two single-ended Op-Amps and connect them in a bridge configuration. You must design a current reference for the system, but you don't have to include the start-up circuit. After you have completed your design, turn in a type written report on what you did to accomplish meeting the following specifications with a 3.3V supply using the 3.3V MOS SPICE models:

$$A_v \geq 110\text{dB},$$

$$f_u \geq 1\text{MHz},$$

$$\text{Phase margin } PM \geq 75^\circ,$$

$$\text{Gain margin } GM \geq 20\text{dB},$$

$$CMRR \geq 110\text{dB @ } 100\text{Hz}, \text{ over the range } \pm 1\text{V from } V_{mid}$$

$$PSRR \geq 106\text{dB @ } 100\text{Hz},$$

$$\text{Input referred Noise: } \frac{v_{in}^2}{\text{Hz}}^{\frac{1}{2}} \leq 350\text{nV}/\sqrt{\text{Hz}} \text{ @ } 10\text{Hz},$$

$$\frac{v_{in}^2}{\text{Hz}}^{\frac{1}{2}} \leq 8\text{nV}/\sqrt{\text{Hz}} \text{ @ } 1\text{MHz},$$

Output swing of $5V_{pp}$ differential with a 3.3V supply into the load for THD simulations.

The differential input voltage is $2.5V_{pp}$, therefore there is a system gain of 2.

Total Harmonic Distortion: $THD \leq 0.005\%$ @ 1kHz,

$$THD \leq 0.01\% \text{ @ } 2\text{kHz},$$

$$THD \leq 0.1\% \text{ @ } 20\text{kHz},$$

The load for the op-amp is a resistor in parallel with a capacitor, $R_L \parallel C_L = 32\Omega \parallel 150\text{pF}$ connected differentially at the output for all THD simulations. For all other specs the load is: $R_L \parallel C_L = 32\Omega \parallel 150\text{pF}$ for differential amps; or $R_L \parallel C_L = 16\Omega \parallel 300\text{pF}$ for single-ended amps. All specs **must** be met with the load connected to the op-amp. Run a final simulation with no load to see if your circuit is still stable, if it is not, explain why. The goal of your design is to minimize the current in the op-amp but **meet** the above specs. Secondly try to minimize total gate area. You must design a current reference as part of the complete op-amp. The final report must be typed, use a computer word processor, with ink drawn figures, or better to use a graphics drawing program, including a schematic drawing of your **complete** circuit with all device labeled same as your netlist. All device sizes must either be on the schematic or in a table immediately following the schematic in your report. SPICE analysis of your circuit for all conditions that prove you met all of the specs on the

final circuit. The SPICE print file, showing the netlist and output data, for each simulation and plots of data where possible. Show all equations you used to design your amplifier in your report. Your report must follow the instructions in the `ProjectFormat.txt` file on the web-page.