Switching Noise and Shoot-Through Current Reduction Techniques for Switched-Capacitor Voltage Doubler

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***Abstract*—Switching noise and shoot-through current reduction techniques for switched-capacitor voltage doublers based on cross-coupled structure are presented. The intuitive analysis of the shoot-through current and switching noise generation processes in the doubler is first reported. Break-before-make mechanism is adopted to minimize the shoot-through current, thereby greatly reducing the no-load supply current dissipation and improving the light-load power efficiency of the voltage doubler. In addition, by employing gate-slope reduction technique at the serial power transistor during turn-on, the switching noise of the voltage doubler is significantly lowered.**

Two voltage doublers with and without the proposed circuit techniques have been fabricated in a 0.6-μm CMOS process. Experimental results verify that the total supply current at no-load condition of the proposed voltage doubler is reduced by twofold and its switching noise is decreased by 2.5 times.

***Index Terms*—Break-before-make mechanism, charge pump, dc–dc converter, shoot-through current, switched-capacitor power converter, switching noise, voltage doubler.**

I. Introduction

In RECENT years, switched-capacitor voltage doublers capable of delivering tens of milliampere load current are growing in great demand, as they are mandatory in the power management ICs for battery-powered portable applications. For example, these doublers are widely utilized for providing a higher supply voltage to the general-purpose I/O circuitries in the mobile phone. Among different types of switched-capacitor voltage doublers, the cross-coupled voltage doubler is the most commonly used topology and its circuit implementation is shown in Fig. 1(a) [1]–[5]. The cross-coupled voltage doubler operates at twice the switching frequency such that either the ripple voltage or the size of the load capacitor can be halved. The voltage doubler, which is driven by the two-phase nonoverlapping clock signals as shown in Fig. 1(b), contains a voltage booster circuit with a pair of cross-coupled nMOS transistors (Ml1 and Mr1) and two flying capacitors (C_{f1} and C_{f2}). The use of nMOS transistors provides automatic reverse bias of the junctions. Two serial pMOS transistors Ml4 and Mr4 act as charge-transfer devices to provide an output voltage of approximately $2V_{\rm DD}$.

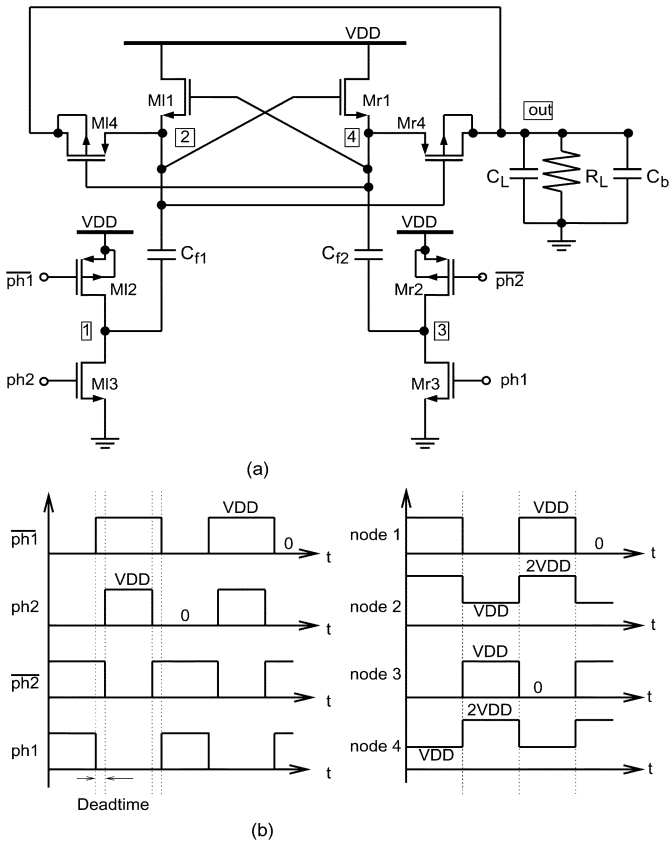

Fig. 1. (a) Circuit diagram and (b) timing diagram of the conventional cross-coupled voltage doubler.

Previous research work on switched-capacitor cross-coupled charge pumps including voltage doublers [1]–[5], mainly targeted at different on-chip applications such as flash memories and EEPROM [1]–[3], mixed-signal integrated systems operated in low-voltage condition [4], or LCD drivers [5]. These charge pumps only need to supply sub-milliampere load current with the use of integrated capacitors. The main aim of the above-mentioned work is to either: 1) ensure reverse bias of the junctions of serial pMOS transistors by using different bulk biasing schemes [2], [3]; 2) reduce device reliability constraint

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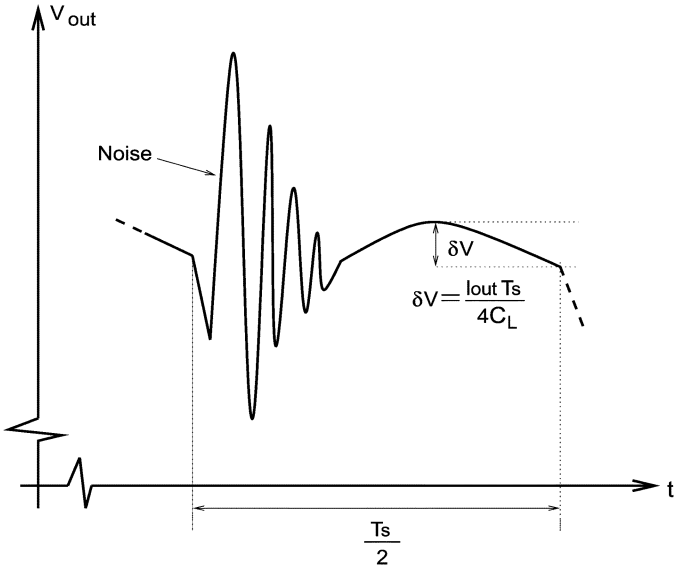

Fig. 2. Close view of the output voltage of the conventional voltage doubler.

at low voltage [4]; or 3) reduce the number of power transistors and capacitors to save chip area [5]. However, in order to allow doublers to deliver tens of milliampere load current, both off-chip capacitors and large power transistors have to be used. The switching of large power transistors is known to generate undesired switching noise [6], [7], especially in switched-mode power converters [8] and CMOS output buffers [9]–[11]. Unfortunately, there is still lack of detailed discussion on the problem associated with the switching noise of the cross-coupled voltage doublers. In fact, in a cross-coupled voltage doubler, the switching noise appears at the output at each half clock period. Generally, the amplitude of the switching noise can be much larger than the ripple voltage (δV) as shown in Fig. 2. The accuracy of the output voltage is degraded by the switching noise. On the other hand, the improper switching of power transistors can generate huge shoot-through current, which is an unwanted power loss. The shoot-through current significantly increases the total supply current and then leads to the degradation of the power efficiency in the cross-coupled voltage doubler especially at no-load and light-load conditions. In order to improve the accuracy and power efficiency of the voltage doubler, circuit techniques to reduce both the switching noise and shoot-through current are critical.

Motivated by the above concerns, both the break-before-make mechanism and the gate-slope reduction technique are proposed in this paper for adoption in the cross-coupled voltage doubler, thereby decreasing both the shoot-through current and switching noise. This paper is organized as follows. The shoot-through current and switching noise generation processes and their design challenges are described in Section II. A simple new voltage doubler to improve both the switching noise and power efficiency is then proposed in Section III, and its operational principle and design issues are also discussed. Experimental results are given in Section IV to verify the improvements of the proposed voltage doubler. Finally, conclusions are given in Section V.

II. Problems of Conventional Cross-Coupled Voltage Doubler

A. Shoot-Through Current Loss

In the conventional cross-coupled voltage doubler, the voltage transitions at nodes 2 and 4 (V2 and V4) shown in Fig. 1(b) cannot be controlled and occurs at the same time during switching. The shoot-through current in the conventional voltage doubler is then associated with the voltage booster circuit (Ml1 and Mr1) and serial power transistors (Ml4 and Mr4) during switching, as their switching activities are determined by V2 and V4.

Due to symmetry of the cross-coupled voltage doubler, the shoot-through current is generated under similar conditions in every half-clock period. Fig. 3 illustrates an example of how the shoot-through current is generated during the increase of V2 from $V_{\rm DD}$ to $2V_{\rm DD}$ and the decrease of V4 from $2V_{\rm DD}$ to $V_{\rm DD}$. The simultaneous transitions of V2 and V4 produce the shoot-through current in four different ways. The first two ways are due to the leakage from power transistors Ml1 and Mr1, respectively. In particular, during the initial phase of clock-signal transitions

$$V_4 - V_2 \geq V_{thn} \text{ and } V_2 > V_{\rm DD} \tag{1}$$

where V_{thn} is the threshold voltage of transistors Ml1 and Mr1. The first shoot-through current leaks from node 2 through Ml1 to the input supply. Without loss of generality, the second shoot-through current flows from node 4 to input supply through Mr1 during the final phase of clock-signal transitions when $V_2 - V_4 \geq V_{thn}$ and $V_4 > V_{\rm DD}$.

In addition, the third and fourth shoot-through currents are generated by the leakage from the output to the input supply due to the simultaneous conduction of transistor pairs (Ml1, Ml4) and (Mr1, Mr4), respectively. The simultaneous conduction depends on the input supply voltage. Fig. 3(b) shows that Ml4 is on when $V_4 \leq 2V_{\rm DD} - |V_{thp}|$ and $V_{\rm DD} > 2|V_{thp}|$. Also based on (1), the minimum input supply to turn on Ml1 and to overlap with the turn-on of Ml4 is $V_{\rm DD} \geq 2|V_{thp}| + V_{thn}$, where $|V_{thp}|$ is the threshold voltage of transistors Ml4 and Mr4. Therefore, the minimum supply voltage for the occurrence of the simultaneous conduction of transistor pairs (Ml1, Ml4) and (Mr1, Mr4) is

$$\begin{aligned} V_{\rm DD} &\geq \max\left(2|V_{thp}|, 2|V_{thp}| + V_{thn}\right) \\ &= 2|V_{thp}| + V_{thn}. \end{aligned} \tag{2}$$

Fig. 3(b) also indicates that the shaded region is the duration of the simultaneous conduction, which appears when the input supply voltage is larger than the threshold voltage of the simultaneous conduction by ΔV. In fact, the shaded region increases with the input supply voltage, thereby increasing both the shoot-through current and unwanted power loss. As a result, the power efficiency of the voltage doubler becomes worse at higher input supply voltages.

B. Switching Noise

As shown in Fig. 2, the switching noise of the voltage doubler consists of the voltage drop and ringing. They are associated

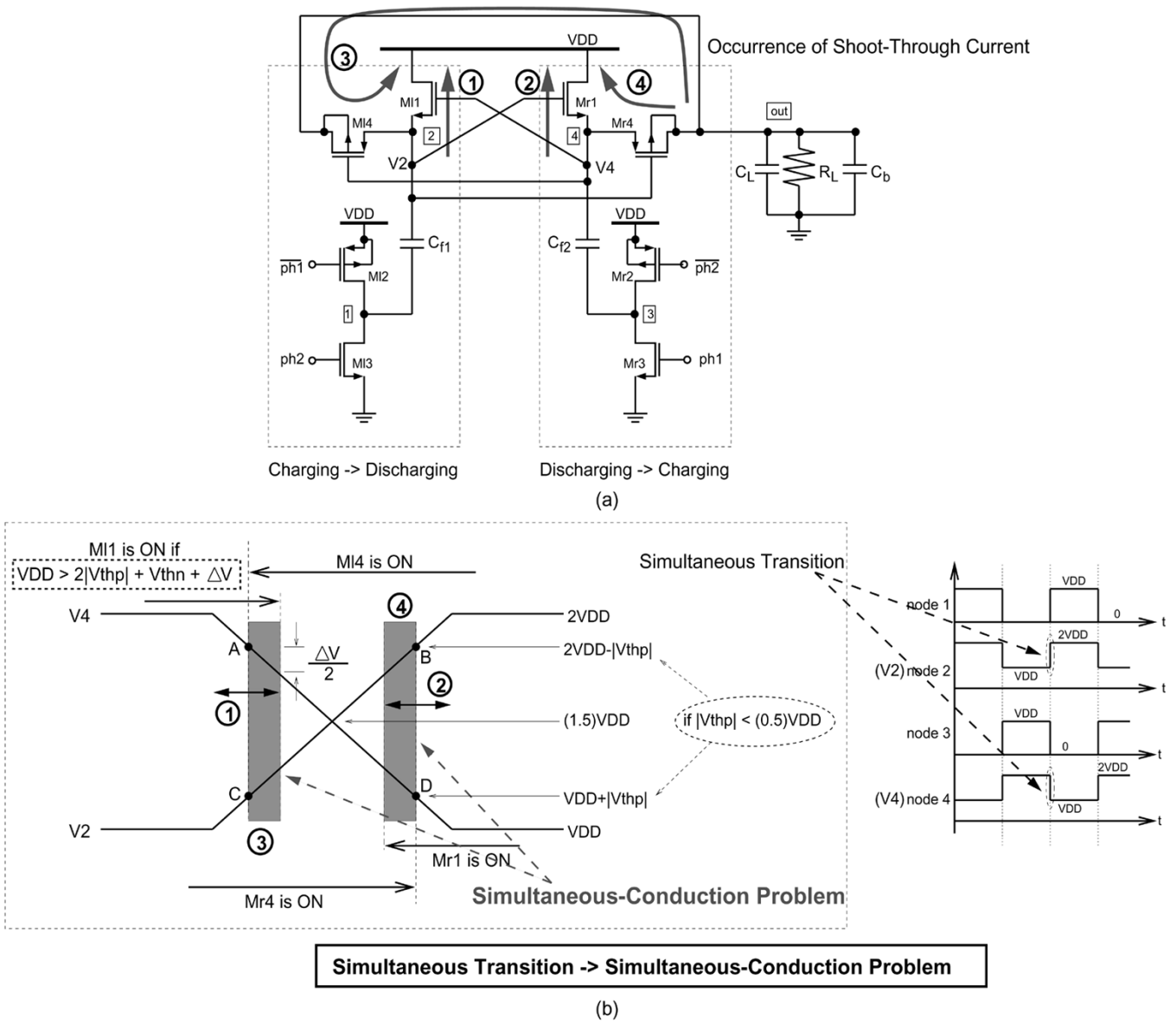

Fig. 3. (a) Shoot-through current generation mechanism in the conventional voltage doubler and (b) its associated reason of occurrence during switching.

with two separate mechanisms. First, the simultaneous conduction problem mentioned before causes the lossy discharge of the output capacitor and leads to the initial output voltage drop during switching. Since the shoot-through current due to simultaneous conduction of (Ml1, Ml4) and (Mr1, Mr4) increases with the input supply voltage, the amplitude of output voltage drop is increased at higher supply voltages, which degrades the accuracy of the voltage doubler.

The switching noise due to ringing appears when one of the flying capacitors (C_{f1} and C_{f2}) is connected to the output. Fig. 4 illustrates an example, in which node voltages V2 and V4 are switching to $2V_{\rm DD}$ and $V_{\rm DD}$, respectively, and the flying capacitor C_{f1} is connecting between the input supply and output through Ml2 and Ml4. The noise source v_n in Fig. 4 is determined by the slopes of the current change (di/dt) in power transistors during switching. Larger di/dt imposes greater noise. Since the size of power pMOS Ml4 is huge and its turn-on is not controlled and fast in the conventional doubler, this leads to large v_n. In addition, a second-order high-frequency *RLC* equivalent circuit is used to study how v_n is transmitted to the output. Since power transistors in the cross-coupled doubler are switched on/off periodically in every half-clock period $(0.5T_s)$, the amplitude of the output switching noise is mainly determined by the gain $v_{\rm out}/v_n$ at even harmonics and up to approximately ten times the switching frequency. Larger high-frequency gain gives rise to larger output noise. Moreover, the noise amplitude at output also depends on the Q value of the *RLC* circuit at high frequencies. Higher Q value results in larger output ringing during switching. Both the high-frequency gain and Q value are determined by R_{ieqv}/R_{oeqv}. When the ratio of R_{ieqv}/R_{oeqv} decreases in the *RLC* equivalent circuit, both the high-frequency gain and Q value are increased and then results in smaller amplitude of the output switching noise. For the voltage doubler delivering tens of milliampere load current, large power transistors are used to achieve low on-resistance, and thus small R_{ieqv} results. This reduces R_{ieqv}/R_{oeqv} and

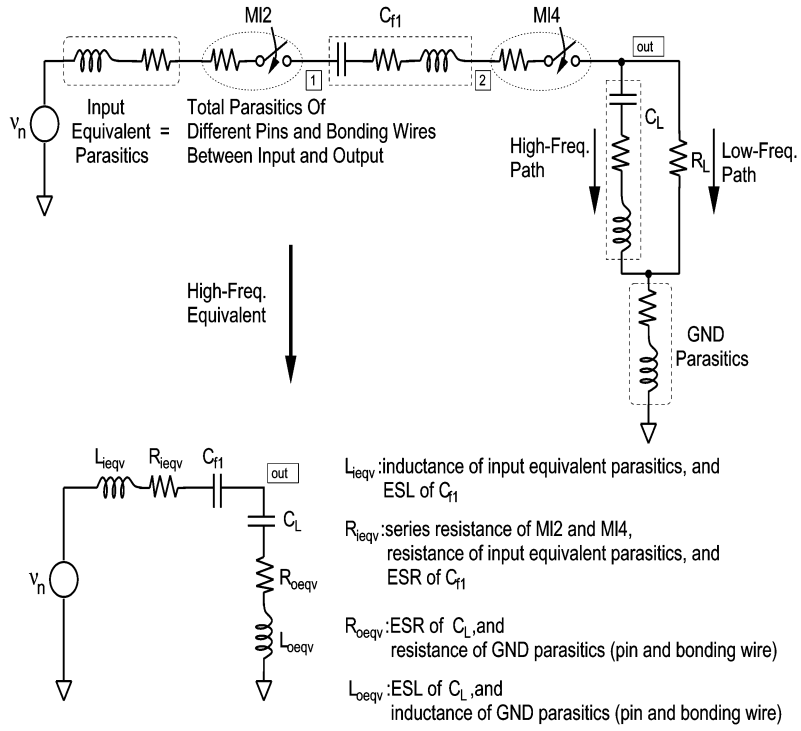

Fig. 4. Equivalent circuit of the voltage doubler when C_{f1} is switching to the discharging phase.

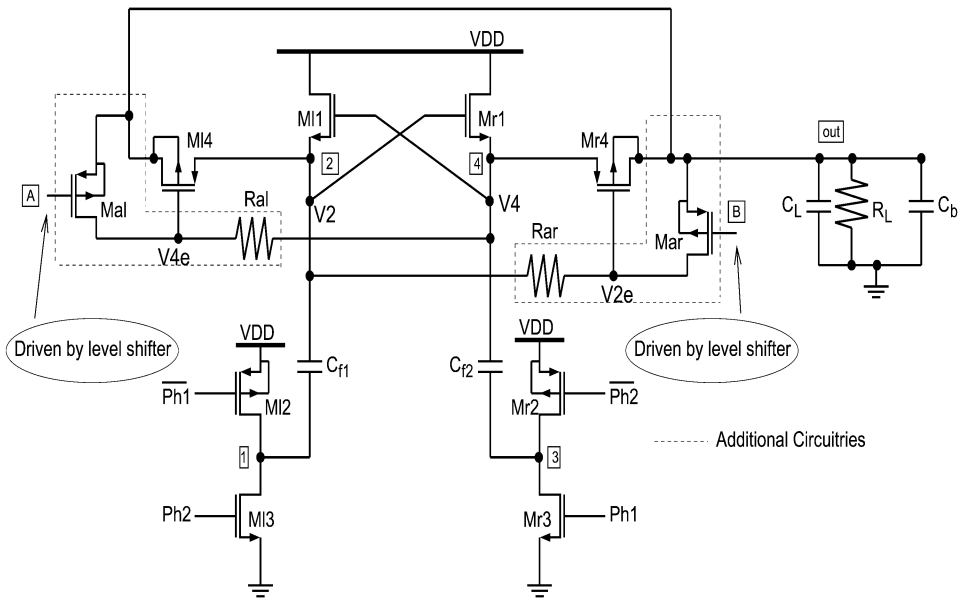

Fig. 5. Core diagram of the proposed voltage doubler.

then increases the amplitude of the switching noise. Both high-frequency gain and Q value with different values of R_{ieqv}/R_{oeqv} are illustrated in Fig. 8. However, it is not power efficient to increase R_{ieqv} by decreasing the size of power transistors since this increases the conduction power loss and eventually lowers the power efficiency of the voltage doubler. On the other hand, a large value ceramic-type load capacitor C_L of tens of microfarad with relatively low equivalent series resistance is adopted to reduce the value of R_{oeqv} and suppress the noise. Similarly, it is also a common practice to use bypass capacitors C_b connected in parallel to C_L to filter out the noise by decreasing the value of R_{oeqv}. However, it is not cost effective to use large-value ceramic-type load capacitors and is impractical to use too many off-chip bypass capacitors as they increase the board space.

III. Proposed Switched-Capacitor Voltage Doubler

From the previous discussion, it is desirable to develop effective circuit techniques in the cross-coupled voltage dou-

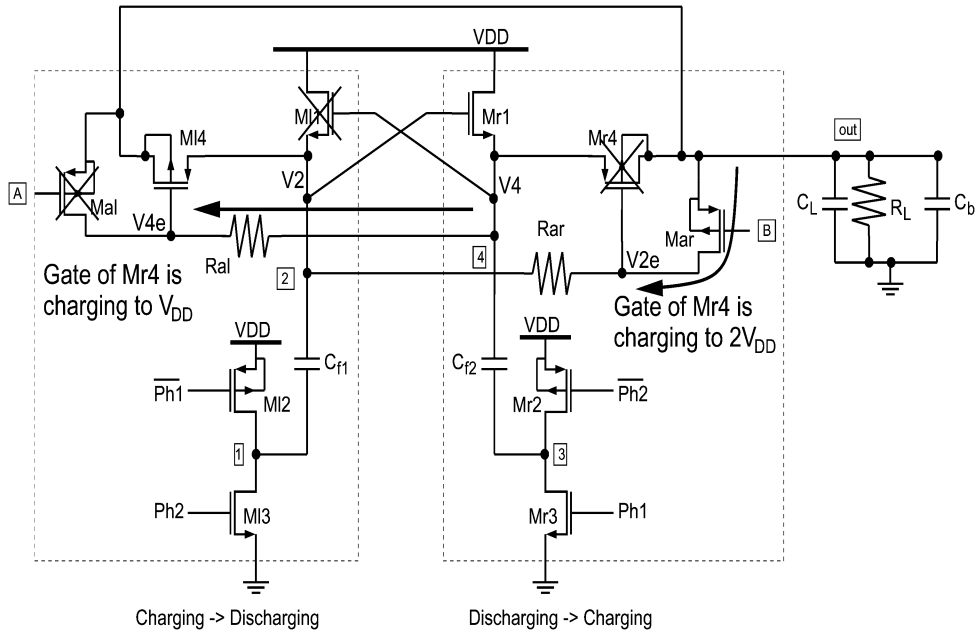

Fig. 6. Operating principle of the proposed voltage doubler.

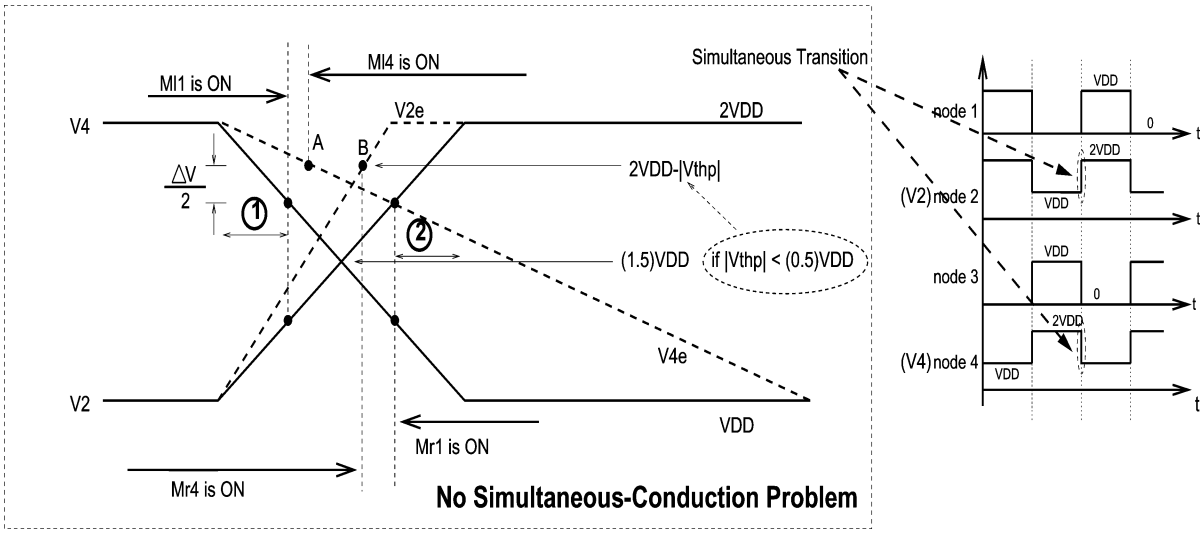

Fig. 7. Simultaneous transitions of clock signals in the proposed voltage doubler.

bler. These techniques are not only capable of reducing the shoot-through current during switching, but also decrease the switching noise at the output. Moreover, the implementation method should be simple to ensure area efficiency.

The new voltage doubler is thus developed to satisfy the aforementioned requirements, and its core circuit is shown in Fig. 5. Two additional poly resistors (Ral and Rar) are placed in series with the gates of serial power transistors Ml4 and Mr4, respectively. In addition, two extra small pMOS transistors (Mal and Mar) are added, which are driven by level shifters to ensure that both Mal and Mar can be turned on and off properly.

A. Principle of Operation

In the proposed voltage doubler, both Mal and Mar only turn on when either of the serial power transistors Ml4 and Mr4 turns off. In particular, transistors Mal and Mar increase the amount of transient current and effectively short the additional resistors. As a result, the gates of power transistors are quickly charged to $2V_{\rm DD}$ and both Ml4 and Mr4 can be turned off much faster. On the other hand, the additional resistors allow power transistors Ml4 and Mr4 to turn on much slower due to the additional *RC* delay. Fig. 6 shows an example of how the additional circuitries operate during switching, in which the gate of Ml4 (V4e) changes to $V_{\rm DD}$ slower due to the delay provided by Ral, and the gate of Mr4 (V2e) switches to $2V_{\rm DD}$ faster because of the additional transient current provided by Mar. As the turn-off process of Mr4 is much quicker than the turn-on process of Ml4, break-before-make mechanism is thus realized. By symmetry, this mechanism also applies to the voltage doubler during switching in the next half clock cycle. Fig. 7 shows the simultaneous transitions of V2, V4,

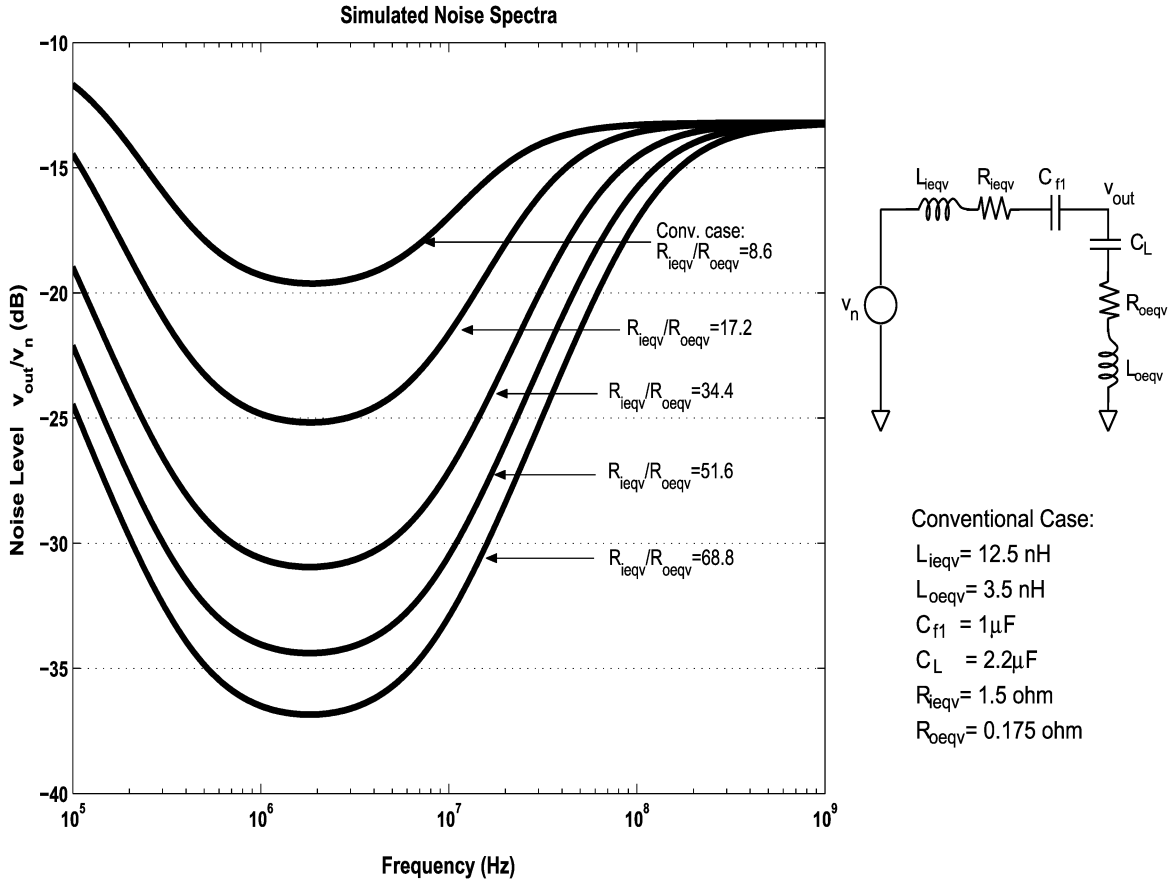

Fig. 8. Simulated $v_{\rm out}/v_n$ spectra of voltage doublers.

V2e, and V4e in the proposed voltage doubler and verifies that simultaneous conduction problem is solved by adopting the break-before-make mechanism. As a result, the shoot-through current can be decreased, thereby reducing the total supply current dissipation and improving the light-load power efficiency of the voltage doubler. In addition, the switching noise due to the output voltage drop can be significantly reduced by minimizing the lossy discharge of the load capacitor during switching.

Moreover, the use of the additional resistors reduces the slope change of the gate voltage of the serial power transistors Ml4 and Mr4 when either of them is turning on. The di/dt noise associated with the switching of Ml4 or Mr4 is reduced, as the current change of Ml4 or Mr4 is slower. The value of v_n is thus decreased. In addition, the dynamic resistance of Ml4 and Mr4 is increased during turn-on, so both the value of R_{ieqv} and the ratio of R_{ieqv}/R_{oeqv} become greater. Fig. 8 demonstrates the comparison of the $v_{\rm out}/v_n$ spectra between the conventional and proposed voltage doublers. The increase in R_{ieqv}/R_{oeqv} in the proposed voltage doubler decreases both the high-frequency gain and Q value of the *RLC* equivalent circuit. As a result, the switching noise due to ringing is significantly reduced in the proposed voltage doubler. It should be also noted that the static resistance of Ml4 and Mr4 is unchanged so no conduction power loss in the voltage doubler is increased. Therefore, both low switching noise and high power efficiency can be achieved simultaneously in the proposed voltage doubler.

B. Design Considerations

It is critical to design the appropriate size of Mal, Mar and values of Ral, Rar for reducing both the shoot-through current and switching noise in the proposed voltage doubler. The break-before-make mechanism provides the following guideline:

$$\frac{C_g}{\mu_p C_{\rm ox}(W/L)_{\rm Mar,Mal}(2V_{\rm DD}-|V_{thp}|)}\ln\left(\frac{19V_{\rm DD}-10|V_{thp}|}{3V_{\rm DD}-2|V_{thp}|}\right) \ll \sum_{i=1}^{N} C_i(R+\sum_{j=1}^{i} R_j) \le 0.05T_s \quad (3)$$

where C_g is the gate capacitance of serial power transistor Ml4 or Mr4, $(W/L)_{\rm Mar,Mal}$ is the size of additional transistors Mal and Mar, R is value of Ral and Rar, and T_s is the clock period. The first term of (3) provides the time required to turn off Ml4 and Mr4 relating to the size of additional transistors. In particular, during the turn-off process of either Ml4 or Mr4, the corresponding Mal or Mar operates in the triode region. The first term of (3) can then be derived by assuming either Mal or Mar is on when the gate of power transistor Ml4 or Mr4 is changing from $V_{\rm DD}$ to $0.9V_{\rm out}$ and $V_{\rm out}=2V_{\rm DD}$. It should also be noted that the size of Mal and Mar should be determined when the doubler is operating in the lowest input supply voltage, which gives the maximum break time of Ml4 and Mr4. In addition, by modeling the power transistor Ml4 or Mr4 with a cascaded N-stage *RC* chain, in which the components of each stage being R_i and

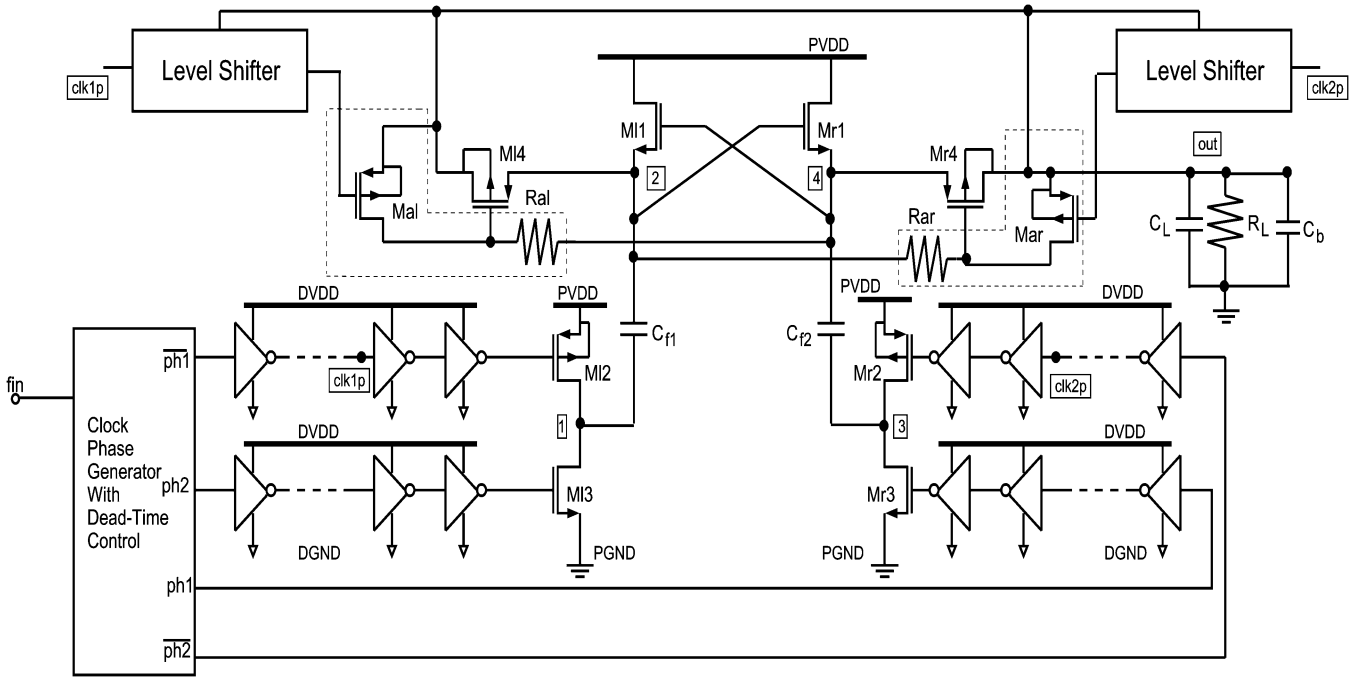

Fig. 9. Schematic of the proposed voltage doubler.

C_i, the Elmore delay of turning on Ml4 or Mr4 is then given by the middle term of (3) [12]. Therefore, the value of R can be designed to maximize the Elmore delay. The lower bound of the Elmore delay ensures the break-before-make mechanism and its upper bound should be at least ten times smaller than half of the clock period. The matching of additional resistors Ral and Rar only affects the symmetry of the output switching noise in a clock period. Both switching noise and shoot-through current can still be decreased with imperfect matching of Ral and Rar. Simulations verify that with $\pm 15\%$ variation of poly resistors of Ral and Rar [13], both switching noise and shoot-through current can still achieve twofold reduction.

C. Circuit Implementations

Fig. 9 shows the schematic of the proposed voltage doubler [14]. The anti-phase nonoverlapping clock signals are generated by the dead-time circuit and then passed through the digital buffers realized by the inverter chains to drive power transistors Ml2, Ml3, Mr2, and Mr3. These clock signals minimize the shoot-through current passing through transistor pairs (Ml2, Ml3) and (Mr2, Mr3), during transients in order to improve the power efficiency of the voltage doubler. Level shifters shown in Fig. 10 are used to convert the voltage level of the logic signals of the digital buffers from $V_{\rm DD}$ to $V_{\rm out}$. The gate of the additional transistors Mal and Mar can then be driven by level shifters with the voltages ranging from 0 to $2V_{\rm DD}$ to ensure Mal and Mar turn off properly. In addition, the size of both Mal and Mar can be minimized to save chip area. In our design, the size of Mal and Mar is 75 times smaller than that of power transistors Ml4 and Mr4.

D. Design Extension

Both proposed techniques, the break-before-make mechanism and the gate-slope reduction technique, are not limited to the cross-coupled voltage doubler. They can also be applied to other cross-coupled charge pumps. As an example, Fig. 11 shows a $2^n\times$ charge pump using cascading N-stage cross-coupled voltage doubler in series, in which each doubler adopts the proposed circuit techniques. Since the supply voltage of each doubler keeps increasing, both shoot-through current and switching noise become worse in the $2^n\times$ charge pump if the proposed techniques are not used. Therefore, it is more effective to adopt the proposed design techniques in the $2^n\times$ charge pump such that both the shoot-through current and switching noise can be greatly reduced simultaneously.

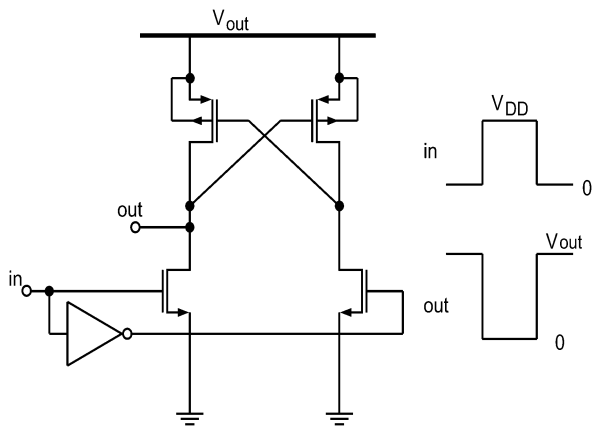

Fig. 10. Circuit diagram of the classical level shifter.

IV. Experimental Results

To verify the functionality of the proposed voltage doubler and compare its performance with that of the conventional counterpart, both the proposed and conventional voltage doublers

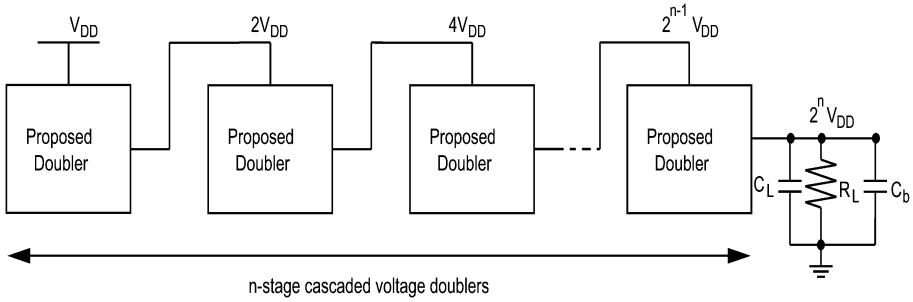

Fig. 11. Schematic of $2^n\times$ charge pump.

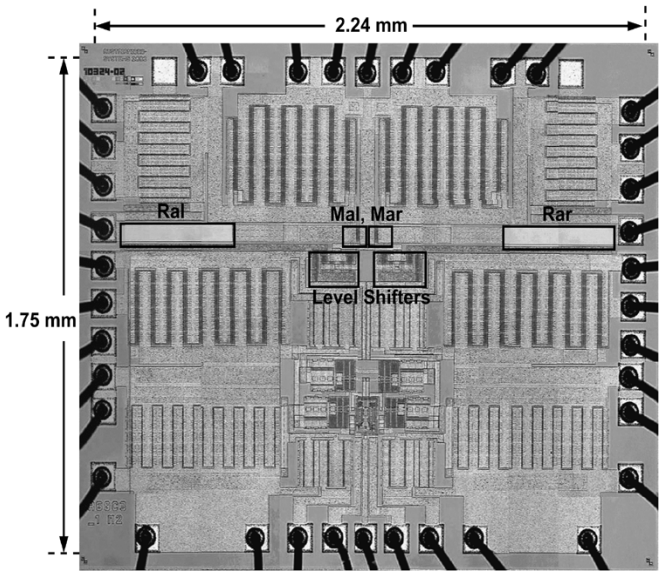

Fig. 12. Micrograph of the proposed voltage doubler.

have been implemented with a standard 0.6-μm CMOS n-well process. Layout arrangements of both conventional and proposed voltage doublers are the same except the additional circuitries in the proposed doubler. Fig. 12 shows the micrograph of the proposed voltage doubler and its size including all the pads is 3.92 mm^2. Additional resistors, transistors, and level shifters in the proposed doubler only increase the chip area by 3.98% compared with the conventional counterpart.

A. DC Output Voltage and Switching Noise

Both voltage doublers are supplied with an input voltage ranging from 1.5 to 2.5 V, operating at the switching frequency of 500 kHz, and delivering a load current up to 50 mA; therefore, they can be used in the power management system of the battery-powered portable applications. Fig. 13 shows the measured output voltage of the proposed voltage doubler for different supply voltages. The results indicate that the voltage doubler can properly double different input supply voltages. The measured output ripple voltages of the proposed and conventional voltage doublers under different supply voltages and loading conditions are compared in Figs. 14 and 15. The results demonstrate that the amplitude of the switching noise is relatively independent of the loading current, as they are high-frequency noises. By reducing the gate-slope change of

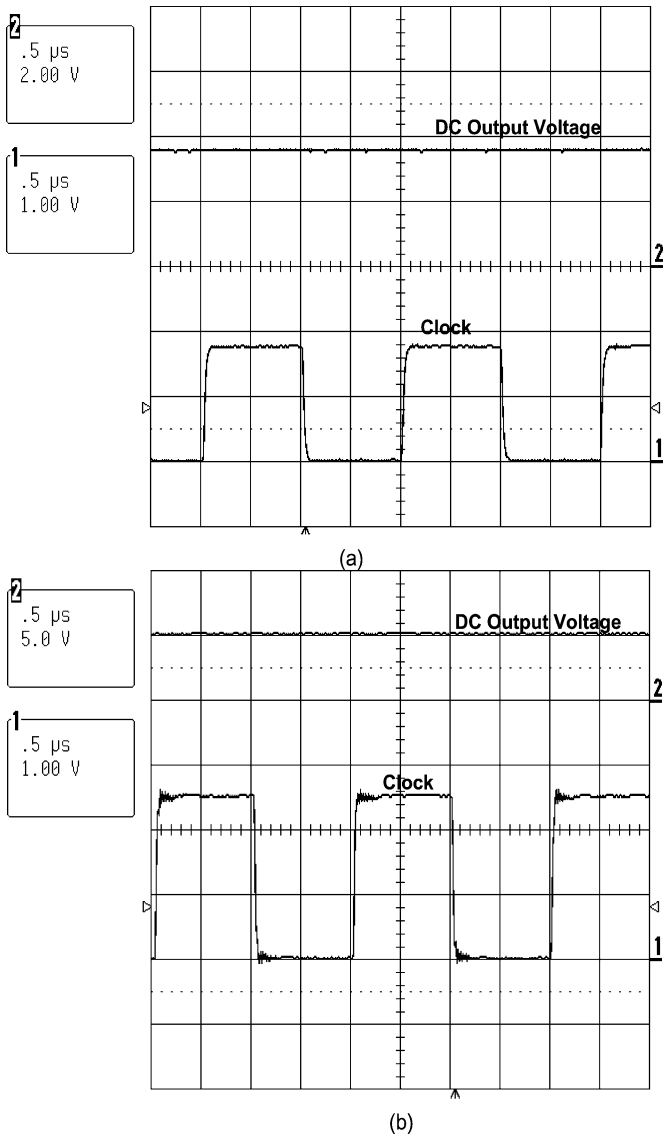

Fig. 13. Measured output voltages of the proposed voltage doubler at (a) $V_{\rm DD} = 1.8$ V and (b) $V_{\rm DD} = 2.5$ V.

the serial power transistors during turn-on, it is verified that both the ringing and noise amplitude are greatly decreased in the proposed voltage doubler with different input supply voltages. In particular, Table I shows that the glitch amplitude of the proposed voltage doubler has been reduced by 2.5 times as compared to that of the conventional doubler. Fig. 16 demonstrates the output noise spectra of the conventional

TABLE I
PERFORMANCE SUMMARY OF THE MEASUREMENT RESULTS

	Conventional Voltage Doubler	***Proposed Voltage Doubler***
Technology	AMS 0.6-μm CMOS process	
Flying Capacitor (C_{f1}, C_{f2})	1 μF	
Load Capacitor (C_L)	2.2 μF	
Bypass Capacitor (C_b)	220 nF	
Switching Frequency (f_s)	500 kHz	
Load Current (I_L)	≤ 50 mA	
Input Voltage Range (V_{DD})	1.5 V – 2.5 V	
Quiescent Current	1.52 mA @ V_{DD} = 1.8 V 3.27 mA @ V_{DD} = 2.5 V	***1.22 mA @ V_{DD} = 1.8 V*** ***1.63 mA @ V_{DD} = 2.5 V***
Maximum Power Efficiency	93.8% @ V_{DD} = 1.8 V 93% @ V_{DD} = 2.5 V	***95.2% @ V_{DD} = 1.8 V*** ***95.7% @ V_{DD} = 2.5 V***
Maximum Output Noise	30 mV @ V_{DD} = 1.8 V 56 mV @ V_{DD} = 2.5 V	***12 mV @ V_{DD} = 1.8 V*** ***22 mV @ V_{DD} = 2.5 V***
Chip Area	3.77 mm^2	3.92 mm^2

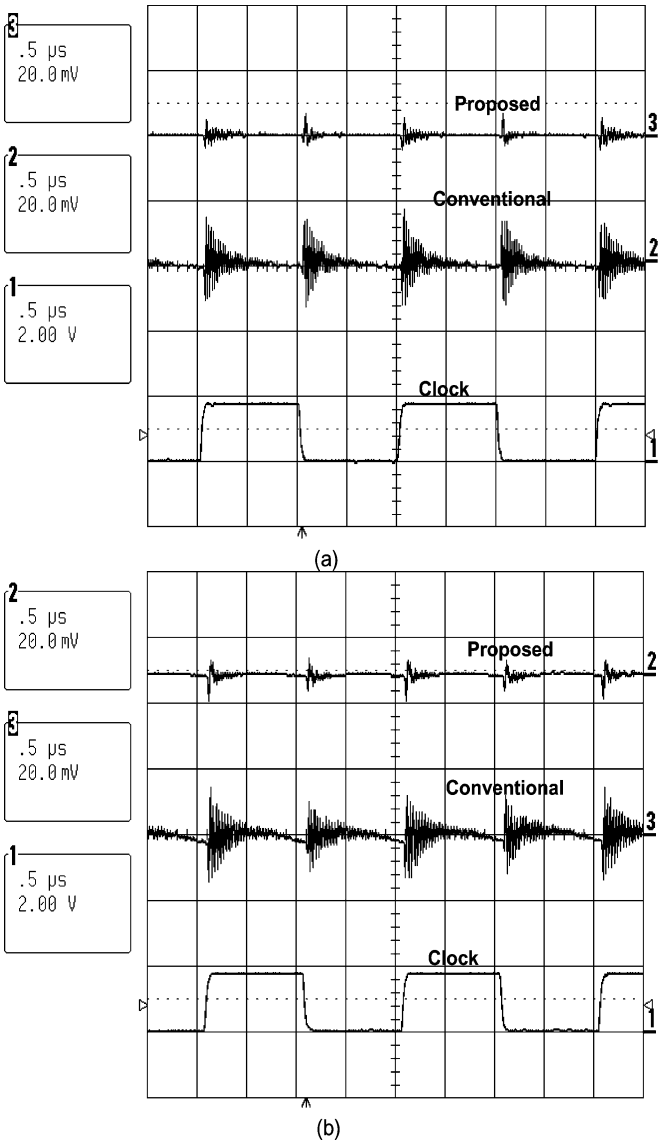

Fig. 14. Measured output-ripple voltages of the voltage doublers at $V_{\rm DD} = 1.8$ V with (a) no load condition and (b) $I_L = 25$ mA.

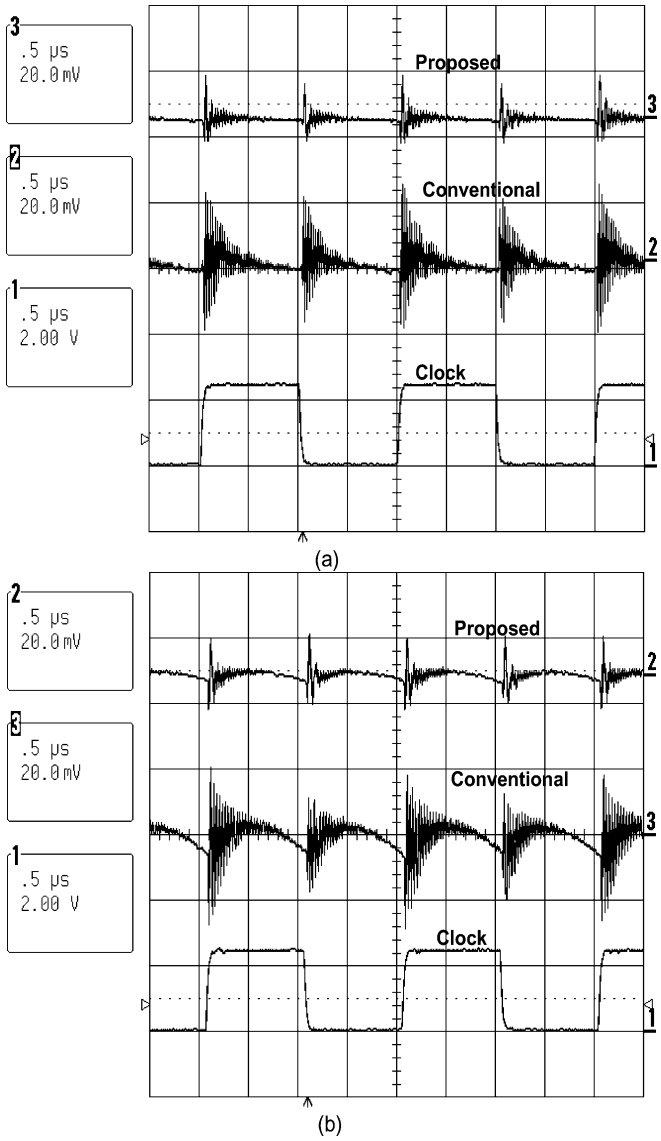

Fig. 15. Measured output-ripple voltages of the voltage doublers at $V_{\rm DD} = 2.5$ V with (a) no load condition and (b) $I_L = 50$ mA.

and proposed voltage doublers. Comparing with conventional design, the amplitude of output pulses at 2nd, 4th, 6th, 8th, 10th, and 12th harmonic of switching frequency in the proposed doubler is decreased by at least 8 dB. This justifies the

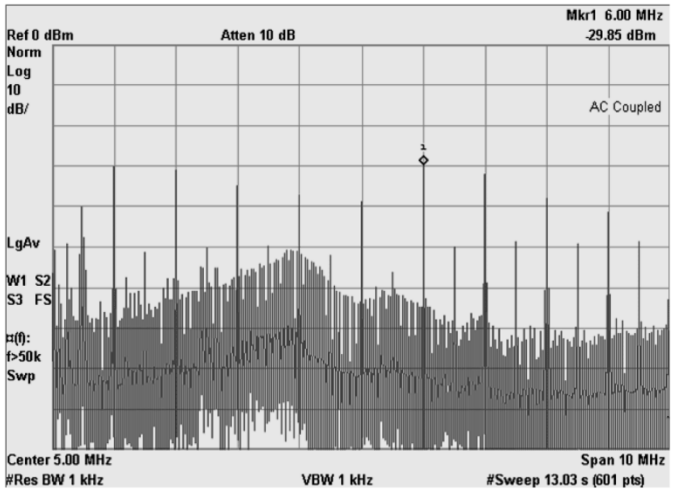

Fig. 16. Output spectra of (a) conventional and (b) proposed voltage doublers with $V_{\rm DD} = 2.5$ V, $f_s = 500$ kHz and $I_L = 5$ mA.

effectiveness of the proposed voltage doubler on the reduction of the output noise spectrum.

B. Quiescent Current and Power Efficiency

Fig. 17 shows the measured quiescent current versus input supply voltage of both conventional and proposed voltage doublers. The quiescent current is the total supply current of the voltage doubler at no-load condition, and is dominated by the shoot-through current and switching current loss at high switching frequencies such as 500 kHz. The quiescent current dissipation in the proposed voltage doubler is much smaller than that in the conventional counterpart under different supply voltages. In particular, the quiescent current of the proposed doubler achieves twofold reduction when the supply voltage is 2.5 V. In addition, the rate of quiescent current dissipation in the proposed doubler increases much slower than that of the conventional counterpart when the supply voltage increases. This verifies that the proposed break-before-make mechanism successfully reduces the shoot-through current in the voltage doubler and its reduction becomes larger at higher input supply voltages.

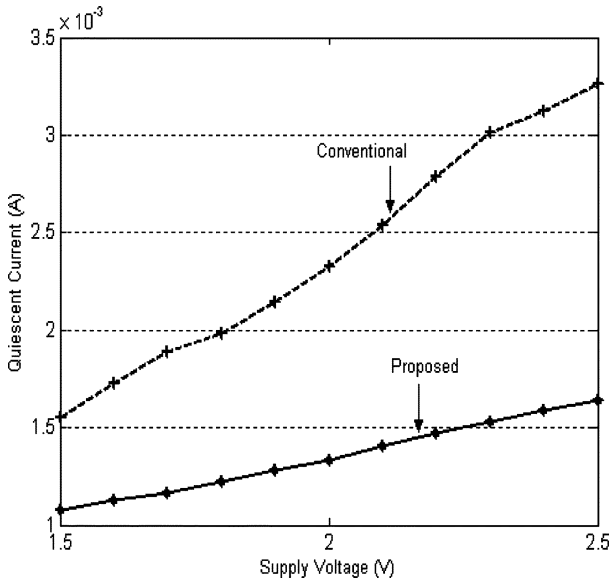

Fig. 17. Measured quiescent current versus input supply voltage of voltage doublers at $f_s = 500$ kHz.

Fig. 18(a) and (b) show the power efficiency of voltage doublers at the supply voltages of 1.8 and 2.5 V, respectively. The power efficiency of the proposed doubler is larger than that of the conventional counterpart in all loading-current conditions. The maximum power efficiency of the proposed doubler is improved by 1.4% and 2.7% at the supply voltages of 1.8 and 2.5 V, respectively. At light-load conditions, the improvement of the power efficiency in the proposed voltage doubler is more significant as the power efficiency is dominated by the switching loss and shoot-through current loss. In fact, it is verified that by reducing the shoot-through current loss in the proposed doubler, the power efficiency at the load current of 5 mA is increased by about 6% and 10% when the supply voltages are 1.8 and 2.5 V, respectively. Therefore, the proposed break-before-make mechanism is efficient in improving light-load power efficiency.

V. Conclusion

Switching noise and shoot-through current reduction techniques for the cross-coupled voltage doubler capable of delivering 100-mW output power in power-management applications are presented in this paper. Both shoot-through current and switching noise generation mechanism in the conventional cross-coupled voltage doubler have been addressed. Simple circuit techniques based on the break-before-make mechanism and the gate-slope reduction technique have been proposed in the cross-coupled voltage doubler. Experimental results demonstrate that the proposed voltage doubler significantly reduces the switching noise and shoot-through current compared with the conventional counterpart. Therefore, low noise, low quiescent current, and high light-load power efficiency can be achieved simultaneously in the cross-coupled voltage doubler with the proposed circuit techniques. The proposed techniques

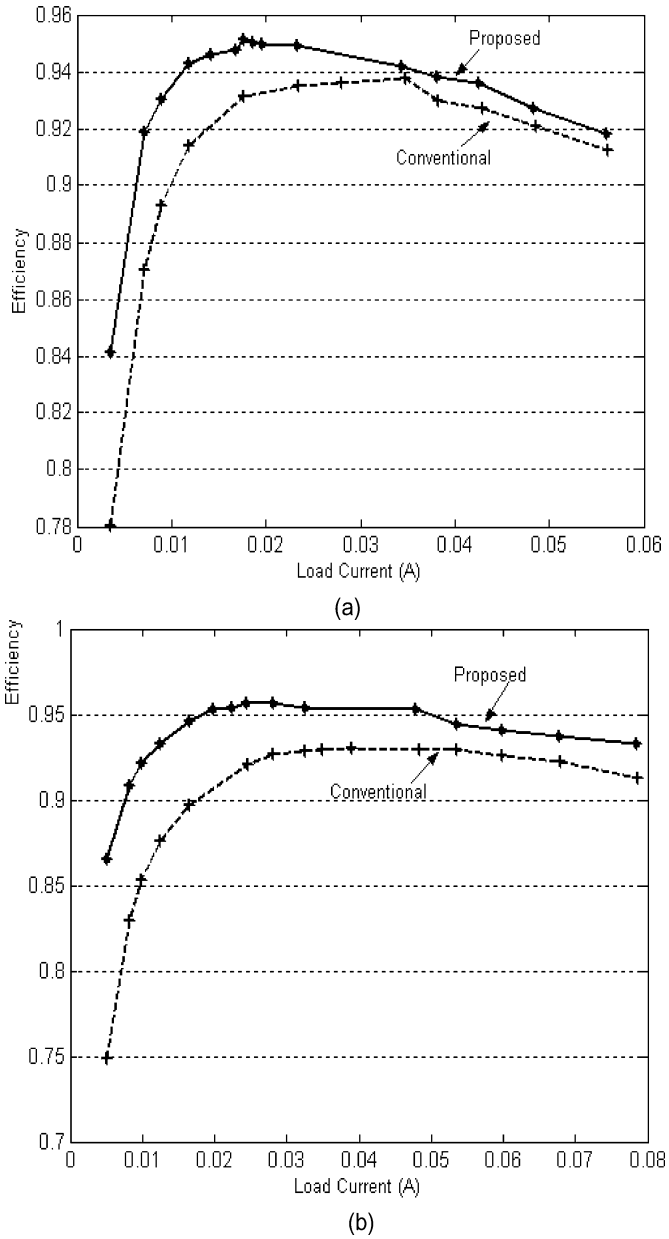

Fig. 18. Measured power efficiency versus load current of voltage doublers when the supply voltage is (a) 1.8 V and (b) 2.5 V.

can also be extended to $2^n\times$ charge pump when the charge pump is formed by cascading n cross-coupled doublers.

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