Magnetoresistance Implications for Complementary Magnetic Tunnel Junction Logic (CMAT)

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***Abstract*— This concept paper provides a first quantitative analysis of complementary magnetic tunnel junction logic (CMAT), a novel cascaded logic family composed solely of magnetic tunnel junctions (MTJs). CMAT is a non-volatile logic family driven by field-induced spin-switching that was inspired by CMOS. A compact CMAT multiplexer is presented, and the impact of magnetoresistance on its behavior is analyzed. The efficiency of CMAT is shown to be a function of the MTJ magnetoresistance, providing impetus for further development of MTJs for computing applications.**

Keywords—spintronic logic, magnetic tunnel junction, beyond-CMOS computing, non-Von Neumann architecture

I. Introduction

Spintronics provides the potential for efficient computing circuits that exploit electron spin, but many proposed spintronic logic families do not permit the direct cascading of logic gates [1]. It is imperative that a logic family provides the capability to cascade switching devices [2] as in [3]–[7], as some combination of additional amplification, control logic, and conversion stages are otherwise necessary [8]. These processes require additional circuit elements such as CMOS transistors that consume significant power, processing time, and area, undermining the gains resulting from the use of emerging technologies.

In this work, we present a first quantitative analysis of CMAT, a novel cascaded logic family composed solely of MTJs that form complementary pull-up and pull-down networks [6]. This logic family, described in section II, solves the challenge of direct cascading in spintronic logic circuits while also providing non-volatile data storage. In section III, we present an extremely compact multiplexer circuit and examine the impact of magnetoresistance on its behavior. We conclude in section IV with suggestions for further work and computing implications of our analysis.

II. CMAT Structure

The basic element of CMAT is an MTJ with a control wire. MTJs are used in which one magnetic material is "harder" than the other; that is, a stronger magnetic field must be applied to switch its magnetic polarization. Charge pulses flow through the control wire to create a magnetic field that switches the magnetization of the "soft" ferromagnetic material. By controlling the direction of the charge pulse, the relative magnetizations of the "hard" and "soft" materials can be set to either the low-resistance parallel state or the high-resistance anti-parallel state.

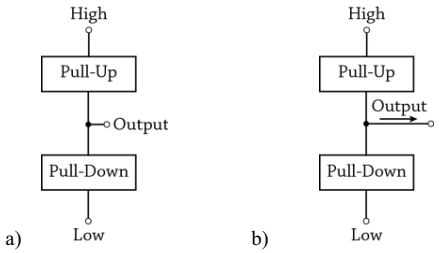

Fig 1. a) CMOS and b) CMAT logic gate structures.

CMAT is structured similarly to CMOS with the FETs replaced by MTJs, as shown in Fig. 1. Charge pulses through the control wire inputs switch the magnetic polarization of the MTJ soft layer; the charge pulses can flow through the control wire in either direction, switching the MTJ to either resistive state. Logic circuits are arranged such that each control wire is an input to one MTJ in the pull-up network and one MTJ in the pull-down network.

As in CMOS, the circuits are designed such that at all times, one of the pull-up and pull-down networks is in a conductive "on" state while the other network is in a resistive "off" state. When an input charge pulse causes MTJs to switch such that the switching networks swap between the "on" and "off" states, charge flows through the MTJs between the supply voltages and the output node until the output node voltage reaches a new steady state.

The simplest CMAT logic gate is the inverter shown in Fig. 2, which outputs a signal with a polarity opposite that of its input. Positive (V_+) and negative (V_-) supply voltages are

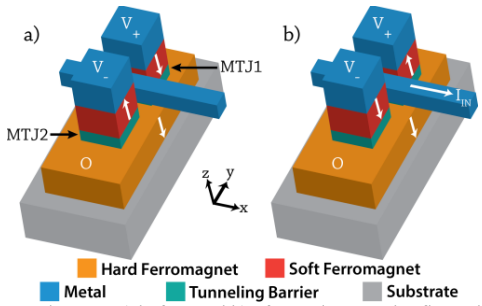

Fig. 2. CMAT inverter a) before and b) after a charge pulse flows through the control current wire [6].

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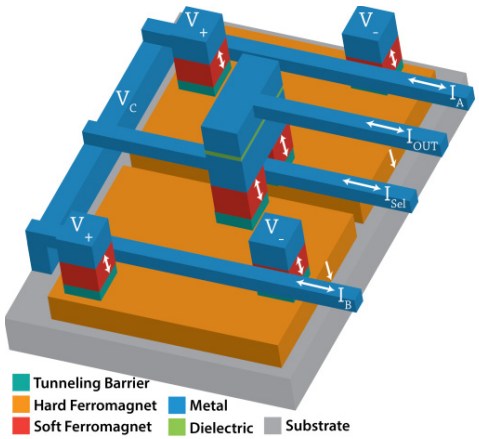

Fig. 3. CMAT 2:1 multiplexer with input currents I_A, I_B, I_{Sel}, and output I_{OUT}.

applied, such that when MTJ1 is in its parallel state and MTJ2 is in its antiparallel state, output node O has a high electric potential. When a charge pulse is asserted in the +x direction through I_{IN}, the magnetization of the soft material in MTJ1 is switched to the +z direction and the magnetization of the soft material in MTJ2 is switched to the -z direction, as shown in Fig. 2b. Node O must therefore reach a low voltage. Through a similar process, a charge pulse in the –x direction through I_{IN} returns node O to the high voltage state. The reader is referred to [6] for further discussion of cascading and basic logic gates.

III. Multiplexer Circuit and Magnetoresistance

The area efficiency of CMAT is evidenced by the two-to-one multiplexer, which is realized with just six MTJs and a single stage of logic in Fig. 3. The *Sel* signal chooses whether the *A* or *B* input value is propagated to the output, with leftward input currents defined as a logical '1' and rightward input currents defined as a logical '0'. Input charge pulses cause the MTJs to switch resistance states, resulting in switching of the output node voltage. As shown in Fig. 4, the output node provides larger voltage swings for large magnetoresistance values. The change in output node voltage causes a charge pulse to flow through the output wire, which can be used as an input current for cascaded logic gates.

MTJs with large magnetoresistance provide the opportunity to operate CMAT circuits with low supply voltages. The worst-case transition, from '001' or '110' to '010' or '101', causes a voltage swing of $0.11\times V_{supply}$ for MR=2, but $0.51\times V_{supply}$ for

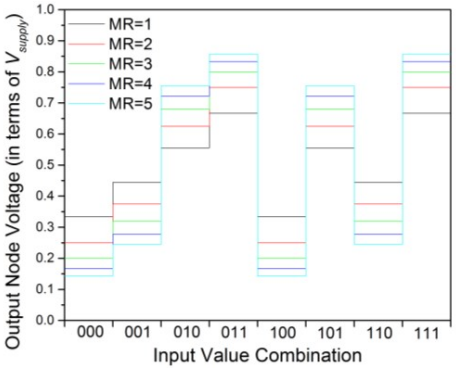

Fig. 4. CMAT multiplexer steady-state waveforms for various magnetoresistance values and input combinations, written as 'I_{Sel} I_A I_B'.

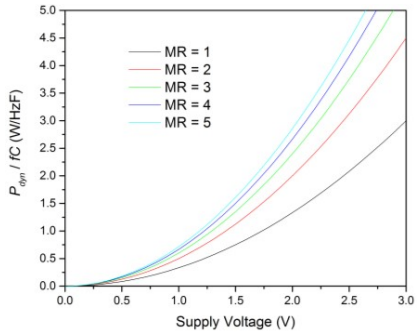

Fig. 5. CMAT dynamic power for various magnetoresistance values and supply voltages (for constant frequency and capacitance).

MR=5. As the output current is proportional to the output node voltage swing, an increase in the magnetoresistance from 2 to 5 provides sufficient current to switch cascaded gates with a five-fold reduction in supply voltage.

CMAT dynamic power dissipation is a complex function of the magnetoresistance, supply voltage, capacitance, and frequency. Fig. 5 shows the effect of magnetoresistance and supply voltage, with small increases in power for magnetoresistance values greater than two. This implies that for large values of magnetoresistance, a reduction in supply voltage translates into a similar decrease in dynamic power dissipation. Though CMAT circuits can overcome small magnetoresistance values with a large supply voltage, MTJs exhibiting large magnetoresistance greatly minimize power dissipation.

IV. Conclusions

CMAT leverages technologies already in common use with MRAM to efficiently perform cascaded logic functions without additional circuit elements. As shown here, the use of MTJs with large magnetoresistance permits the reduction of supply voltage and power dissipation, enabling highly efficient non-volatile logic circuits. These features provide the potential for novel non-Von Neumann architectures that may replace CMOS for general-purpose computing.

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