

InMnAs Magnetoresistive Spin-Diode Logic

Joseph S. Friedman¹, Nikhil Rangaraju², Yehea I. Ismail¹, and Bruce W. Wessels^{1,2}

¹Department of Electrical Engineering & Computer Science

²Department of Materials Science & Engineering

Northwestern University

Evanston, IL, USA

jf@u.northwestern.edu, nikhilrangaraju2011@u.northwestern.edu, ismail@eecs.northwestern.edu,
b-wessels@northwestern.edu

ABSTRACT

Electronic computing relies on systematically controlling the flow of electrons to perform logical functions. Various technologies and logic families are used in modern computing, each with its own tradeoffs. In particular, diode logic allows for the execution of logic with many fewer devices than complementary metal-oxide-semiconductor (CMOS) architectures, which implies the potential to be faster, cheaper, and dissipate less power. It has heretofore been impossible to fully utilize diode logic, however, as standard diodes lack the capability of performing signal inversion. Here we create a binary logic family based on high and low current states in which the InMnAs magnetoresistive semiconductor heterojunction diodes implement the first complete logic family based solely on diodes. The diodes are used as switches by manipulating the magnetoresistance with control currents that generate magnetic fields through the junction. With this device structure, we present basis logic elements and complex circuits consisting of as few as 10% of the devices required in their conventional CMOS counterparts. These circuits are evaluated based on InMnAs experimental data, and design techniques are discussed. As Si scaling reaches its inherent limits, this spin-diode logic family is an intriguing potential replacement for CMOS technology due to its material characteristics and compact circuits.

Categories and Subject Descriptors

B.7.1 [Integrated Circuits]: Types and Design Styles—*Advanced technologies*

Keywords

Spin-diode, spintronics, diode logic, magnetoresistance.

1. INTRODUCTION

As transistor size continues to decrease, predictions for the end of scaling Si transistors continue to be postponed. It is of critical importance, however, to develop new device technologies that will provide further computing improvements over the long term. Furthermore, these new technologies complement CMOS in niche applications such as high performance circuits. These technologies include devices derived from single-electron transistors [1], carbon nanotubes [2] and related graphene

Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. To copy otherwise, to republish, to post on servers or to redistribute to lists, requires prior specific permission and/or a fee.

GLSVLSI'12, May 3–4, 2012, Salt Lake City, Utah, USA.

Copyright 2012 ACM 978-1-4503-1244-8/12/05 ...\$10.00.

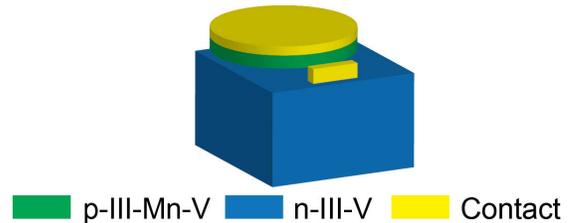


Figure 1. Magnetoresistive spin-diode.

structures [3], [4], nanowires [4], [5], and molecular switches [6]. Additionally, there has been significant interest in devices and logic design techniques that utilize electron spin [7]–[17].

One spintronic device of particular interest is the magnetoresistive spin-diode, which is produced by doping a semiconductor p-n junction with an element that interacts strongly with a magnetic field. A common dopant element is Mn. In this semiconductor heterojunction, shown in Fig. 1, Mn is added to form the paramagnetic p-type layer. The spin-diode acts as a conventional diode in the presence of zero or low magnetic fields, with a high ratio of forward current to reverse current. However, when a magnetic field is applied across the junction, there is an increase in resistivity [12]. Thus, under forward bias, it is possible to define two distinct states: a resistive state in the presence of a magnetic field, and a conductive state in its absence.

Logic styles and circuit architectures should be reconsidered in order to fully utilize new materials and devices. While CMOS transistors and logic have dominated Si-based circuits [18], other devices and logic families exhibit significant advantages. Diode logic is elegant in several respects, such as simple OR gates and single junction devices that allow for compact circuit structures. Circuits based on diode logic use fewer devices than their CMOS counterparts, and therefore potentially consume less power and area while operating at higher speeds. Diode logic, however, has historically been impractical due to the inability of a diode to act as an inverter [19]. As inversion is a necessary function of a complete logic family, standard diodes can only perform complex logic functions in concert with transistors.

The recent invention of the magnetoresistive spin-diode solves this problem, as it allows for the creation of a complete logic family composed solely of spin-diodes, including an inverter [20]. This diode logic family performs logical functions with significantly fewer devices than CMOS, and is therefore a potential replacement for Si CMOS computing. The rest of this paper is organized as follows: the logic family is explained in section 2. In section 3, compact spin-diode logic circuits are discussed, and simulation results are presented in section 4. The computing implications of this diode logic family are discussed in section 5. The paper is concluded in section 6.

2. SPIN-DIODE LOGIC FAMILY

The spin-diode logic family presented in [20] executes logic functions by passing an electric current through spin-diodes to control a magnetic field through other spin-diodes. This logic family is composed solely of spin-diodes; no transistors are required. It is therefore the first example of a complete diode logic family. As such, it provides the simplicity advantages of a two-terminal device structure while exploiting the efficiencies of diode logic.

2.1 Digital States

In this spin-diode logic family, a digital '1' is defined as the "high" current produced by the spin-diode conductive state and a digital '0' is defined as the "low" current produced by the resistive state. Each spin-diode is forward biased, with the positive and negative terminals connected, respectively, to the power supply, V_{DD} and ground. The wires that form these connections are routed to control the magnetoresistance of other spin-diodes. A spin-diode propagating a '1' thus creates a magnetic field in another spin-diode, while a spin-diode propagating a '0' does not.

A metal wire or wires can be placed parallel to the plane of the junction, isolated by an insulator. These wires control the magnetoresistive state of the diode, as currents through the wires create magnetic fields perpendicular to the plane of the junction. Under zero or small field, the diode is in its conductive state; a large field asserts the diode's resistive state. Depending on the relative direction of the currents, these currents interfere either constructively or destructively. If the currents in the two wires travel in opposite directions, the fields will add, doubly suppressing the diode current; if the currents are in the same direction, the fields will cancel, allowing current to flow through the diode. These features form the building blocks of spin-diode logic.

2.2 Basis Logic Elements

In Fig. 2, each of this family's basis logic elements is illustrated using at most a single diode: an inverter, NOR gate, XNOR gate, and OR gate. In each of these configurations, the positive terminal of the diode is connected to V_{DD} , while the negative terminal is routed through the circuit before eventually being grounded. Therefore, in the absence of current through the various control wires, each of these diodes propagates a '1', and the configuration of the control wires dictates the logical function of each gate.

An inverter, the simplest gate, is shown in Fig. 2a. The input current I_A is routed alongside the diode, and induces a field proportional to its current. If I_A is a '1', the current creates a large magnetic field, thereby reducing the current through the diode, and causing the output current I_O to propagate a '0'. If I_A is a '0', it does not create a sufficient magnetic field through the junction, and a '1' is propagated.

The addition of a second input current I_B results in a NOR or XNOR gate, depending on its relative placement in the circuit, as shown in Figs. 2c and 2e. If the two currents flow in opposite directions, the magnetic fields produced by the currents will be oriented in the same direction. Therefore, if at least one of the two NOR inputs is a '1', the output propagates a '0'; otherwise, the output is a '1'. In the case of the XNOR, each current creates a magnetic field through the diode in the opposite direction. Therefore, if both inputs are '1', there is no net magnetic field through the diode, and a large current flows, propagating a '1'. This single device XNOR gate is significantly more compact than the standard ten device CMOS implementation.

As the magnitude of the currents defines the digital states, an OR gate is constructed simply by combining two wire currents, as shown in Fig. 2g. Therefore, if at least one of the inputs is a '1', the output is a '1'. By placing an OR gate as an input to another

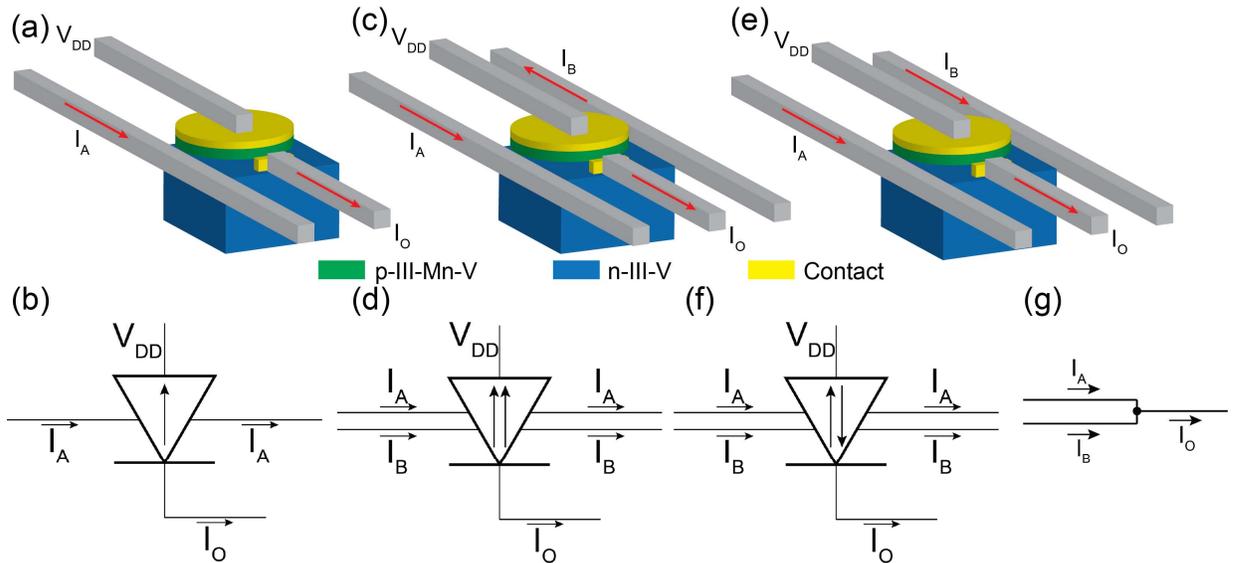


Figure 2. (a) Inverter consisting of input wire with current I_A routed alongside the diode to control the output current I_O . The positive terminal is connected to V_{DD} and the negative terminal is connected to ground. A high input current results in a magnetic field that suppresses the output current. (b) Symbol for spin-diode inverter. (c) Additional input current I_B results in a NOR gate. A high current on either input suppresses the output current. In the case of high currents on both inputs, the output current is doubly suppressed. (d) Symbol for spin-diode NOR gate. (e) Inverting the direction of I_B produces an XNOR gate. In this configuration, a high current on one of the input wires suppresses the output current. Unlike the NOR gate, high currents on both inputs cancel the magnetic fields, allowing a high current to flow through the output. (f) Symbol for spin-diode XNOR gate. (g) OR gate formed by the summation of currents, satisfying the principle of conservation of charge.

gate, a variety of logic functions with more than two inputs can be produced.

3. SPIN-DIODE CIRCUIT DESIGN

These four basis logic elements can be arranged to implement any logical circuit. While the functions are logically equivalent to traditional CMOS circuits, this spin-diode logic family has a starkly different structure.

3.1 Adder

A common circuit is a one-bit full adder, shown in Fig. 3a, which calculates a one-bit sum and carry-out based on the addition of two bits and a carry-in [21]. There are three inputs (A , B , and C_{IN}) and two outputs (C_{OUT} and Sum), optimized for this logic style as

$$C_{OUT} = (A \wedge B) \vee (A \wedge C_{IN}) \vee (B \wedge C_{IN}) \quad (1)$$

$$= \overline{\overline{A \vee B} \vee \overline{A \vee C_{IN}} \vee \overline{B \vee C_{IN}}}$$

$$Sum = A \oplus B \oplus C_{IN} = \overline{\overline{A \oplus B} \oplus C_{IN}} \quad (2)$$

As illustrated in the figure, Sum is generated by cascading two XNOR gates. In XNOR1, A and B are inputs, and in XNOR2, one input is C_{IN} , and the other input is the signal propagated by XNOR1. In both gates, if the two inputs are the same, a '1' is propagated. If the two inputs are different, a '0' is produced. Similarly, C_{OUT} is achieved with three NOR gates, an OR gate, and an inverter. NOR1, NOR2, and NOR3 each propagate a '0' if either input is a '1'; when these propagated currents are summed

in OR1, a '0' is propagated unless at least two of the initial inputs are '0'. This value is inverted to generate C_{OUT} .

3.2 Multiplexer

A two-to-one multiplexer is another useful circuit that can be built with this logic family. As shown in Fig. 3b, INV1 produces an inverted select signal. The select and inverted select signals are routed, respectively, through NOR gates alongside A and B . Each NOR gate propagates a '0' unless a signal with a '0' has been selected. These signals are combined and inverted such that a '1' is propagated unless a signal with a '0' has been selected.

3.3 Latch

This logic family also enables an intriguing and simple latch, shown in Fig. 3c. As seen in the diagram, each NOR latch output is routed to the other NOR input, forcing opposite values to be propagated. When one of the diodes propagates a high current, the current is suppressed in the second diode, which allows the first diode to propagate a high current, thereby maintaining a self-consistent state. To set the value stored in the latch, an external current is passed through one of the diodes. To set a '1', a current is passed through NOR1. To set a '0', a current is passed through NOR2. This circuit is a bistable inverter chain, and can be used to create stable memory storage.

4. CIRCUIT CHARACTERIZATION

This logic family integrates the capability of a current to create a magnetic field with the effect of this field on spin-diode

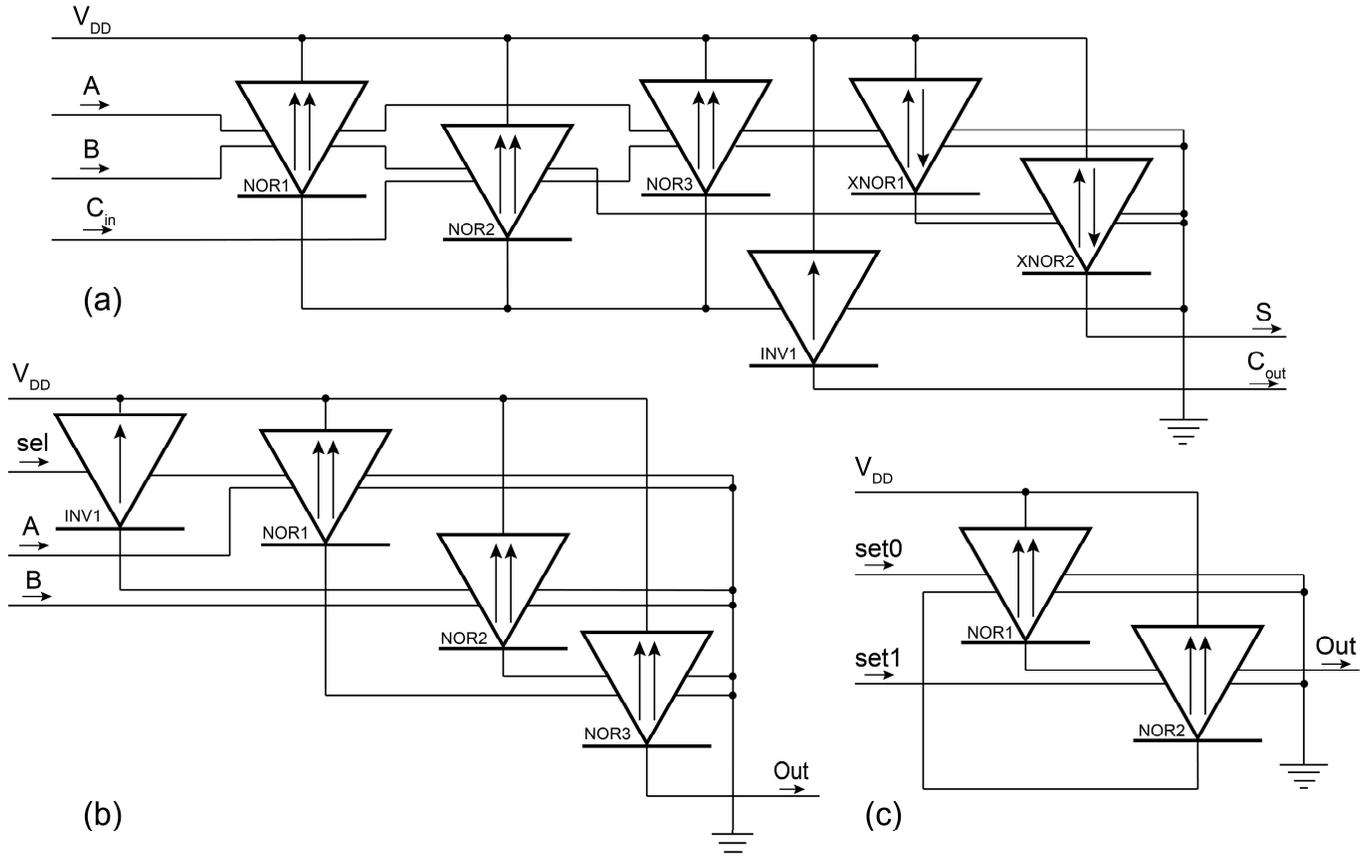


Figure 3. Spin-diode functions: (a) Adder (b) Multiplexer (c) Latch.

current. These phenomena have been evaluated in the context of the circuits discussed in section 3.

4.1 Magnetic Field Strength

Ampere's law can be used to calculate the field created by a current. For a circular line integral, the ratio between the magnetic field B and the current I , in units of T/A, is

$$\frac{B}{I} = \frac{\mu_r \mu_0}{2\pi R} = \frac{2 \times 10^{-7} \mu_r}{R} \quad (3)$$

where R is the distance in meters between the wire and the diode. This ratio is important for signal integrity, as a higher ratio allows for greater control of the magnetoresistive effects of the diode. Prior art indicates that B/I ratios on the order of 25 T/A has previously been achieved, suggesting a radius on the order of 10 nm. This ratio is sufficient for the current from one of these diodes to control the magnetoresistance of another diode.

4.2 InMnAs Diode Characteristics

Magnetoresistive III-Mn-V heterojunction spin-diodes have been fabricated by depositing III-Mn-V magnetic thin films on III-V semiconductor substrates followed by standard photolithographic processes [13], [15]. The response of this diode to the magnetic field exhibits the characteristics necessary to create magnetoresistive diode logic. The diode has the additional outstanding feature of a positive magnetoresistance that persists even at room temperature. As the measurements in Fig. 4 make clear, the current I decreases significantly as the magnetic field is increased. When the voltage is increased, the I_{on}/I_{off} ratio increases, where I_{on} is the zero-field current and I_{off} is the current at a higher field (e.g., 5 T). A high ratio is useful to differentiation between the two digital states. With developments in nanowire technology and other charge-carrying structures, it should be possible to place these currents sufficiently close to the diodes to produce the magnetic fields necessary to cascade diode logic. It is expected that increasing the Mn content of the heterojunction will lead to increased sensitivity to magnetic fields (i.e., increased g-factor), thereby reducing the current, field, power, and area requirements [22]. Operation below room temperature will also reduce the structural requirements of the system [17].

4.3 Circuit Simulation

To implement this logic family, it is necessary to define the magnitude of the '1' and '0' currents as well as V_{DD} . As the InMnAs device functions non-linearly, it is difficult to determine

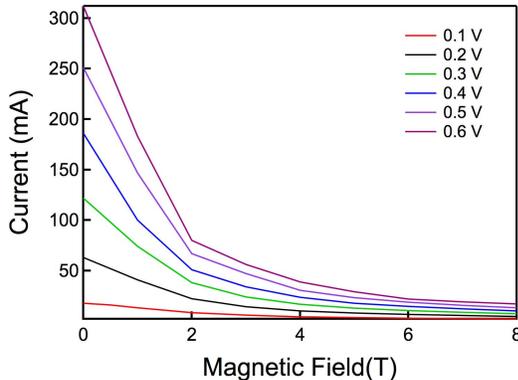


Figure 4. Spin-diode current as a function of magnetic field at various voltage biases [16].

a precise current value to represent '0' and '1', but an approximate value of 32 mA and 160 mA, respectively, is chosen for a V_{DD} of 0.4 V. SPICE models for the basis logic elements have been developed based on the magnetic field calculations and experimental data characterizing the diode. Simulations for the adder, multiplexer, and latch using Synopsys HSPICE are discussed below.

4.3.1 Adder

The signal integrity of this logic family is illustrated in Table 1 for the adder shown in Fig. 3a. As seen in the table, there is a clear differentiation between high and low output currents. Due to the characteristics of the circuit, there are slight variations among the '0' and '1' signals. The values of C_{OUT} make the relationship between the circuit structure and output values particularly clear; the magnitude of C_{OUT} is directly related to the number of '1' inputs. This result agrees with the expected function, as the parallel inputs to INV1 are determined by the sum of the inversion of the input signals. Thus, an increased number of '1' inputs results in a decreased input to INV1 and therefore an increased C_{OUT} current.

Table 1. Adder signal integrity (all currents in mA)

A	B	C	Sum	C_{OUT}
32	32	32	24	15
32	32	160	140	36
32	160	32	186	36
32	160	160	31	97
160	32	32	186	36
160	32	160	31	97
160	160	32	24	97
160	160	160	140	128

4.3.2 Multiplexer

The simulation results for the multiplexer are shown in Table 2. Similar to the adder, the differentiation between the '0' and '1' outputs is sufficient to drive spin-diode logic circuits. In this circuit, the variation in output currents is instructive to the series nature of signal propagation. The input currents to NOR3 are the output currents from NOR1 and NOR2, and NOR2 in turn receives one of its inputs from INV1. The nonlinear behavior of the spin-diode is therefore accentuated by the series connection of these diodes, resulting in an irregular set of output currents.

Table 2. Multiplexer signal integrity (all currents in mA)

Sel	A	B	Out
32	32	32	44
32	32	160	55
32	160	32	106
32	160	160	129
160	32	32	41
160	32	160	112
160	160	32	47
160	160	160	130

4.3.3 Latch

In the simulation shown in Fig. 5, the latch starts in the metastable state, where the outputs of the two NOR diodes are equivalent. As these two diodes drive each other, this situation is stable. When set0 is asserted, NOR1 turns off, allowing NOR2 to turn on. When set0 reverts to '0', the latch continues in a bistable

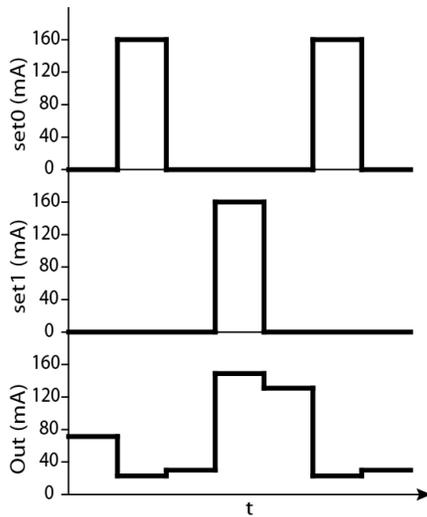


Figure 5. Setting and resetting the spin-diode latch.

state, with NOR1 off and NOR2 on. If set1 is asserted, NOR2 turns off and NOR1 turns on. Once the latch has been switched from the metastable state to a bistable state, the latch will maintain its state until a set signal is asserted.

5. ANALYSIS OF LOGIC FAMILY

5.1 Circuit Design

As the spin-diode has unique properties, such as its power dissipation and fan-out characteristics, the circuit design process must fundamentally change. An analysis of several example circuits demonstrates these design techniques.

5.1.1 Fan-in

Having demonstrated the feasibility of OR and NOR gates with multiple inputs in section 4, it is tempting to consider a gate with an arbitrarily large number of inputs. This scheme, however, is not currently practical, as the ‘0’ current input to the diode is proportional to the number of inputs, and with a sufficiently large number of inputs acts as a ‘1’ current. A device of this sort should therefore be implemented with multiple levels of logic, although this circuit remains far more efficient in terms of area, speed, and power than a comparable CMOS device.

In the adder mentioned above, the output ‘1’ currents produced by Sum are significantly greater than those produced by C_{OUT} . This is caused by the fact that whereas Sum is driven by an XNOR gate, C_{OUT} is driven by the inversion of the sum of three currents. Therefore, since the current in a ‘0’ signal is not sufficiently small to be negligible, the minimum field through INV1 is of a moderate value, whereas the minimum field through XNOR2 is close to zero. The maximum output current from XNOR2 is thus significantly higher than INV1. While this does not cause problems in most spin-diode circuits, signal integrity may be compromised when implementing XOR gates.

5.1.2 Leakage Current

The aforementioned issue is caused by the leakage characteristics of the spin-diodes that have been produced to date [12], [14], [17]. Even in the presence of high magnetic fields, a small leakage current is caused by the imperfect scattering of holes at the p-n junction. Efforts are currently underway to

decrease the leakage current, but it currently poses a complication for spin-diode circuits. Two solutions include:

1) Multiple power supplies: If multiple values of V_{DD} are used and applied separately to different diodes, leakage effects can be mitigated. As the current through a diode is directly related to the voltage across the diode, the current can be enlarged by increasing the V_{DD} connected to a diode. A large V_{DD} should therefore be applied to diodes with a large fan-in, and a small V_{DD} to diodes with a small fan-in. This technique comes at the cost of additional power grid circuitry, but guarantees that the output current of the various diodes will be similar. In the case of the adder circuit, changing V_{DD} for INV1 from 0.4 V to 0.6 V results in output currents more similar to those produced by NOR2.

2) Limited design space: Even after accounting for leakage current, it is possible to construct any logical function with this spin-diode logic family. By creating design rules that prevent certain circuit structures, signal integrity can be ensured. For example, by prohibiting a multiple-input NOR gate from driving an XOR gate, many leakage current issues can be avoided. Another design rule that suppresses the impact of leakage current is to limit the effective number of gate inputs to two.

5.1.3 Fan-out

Another unique aspect of this logic family is the concept of “fan-out.” As an “input” to a device is merely a wire close to a diode, this wire can be used as an input to multiple devices without degrading the signal. This structure is possible because the positive and negative terminals of each diode are directly connected, respectively, through wires to V_{DD} and ground, with no constraint on the wire path or length.

5.1.4 Power Dissipation

The mechanism for consuming power is profoundly different in this logic family. In CMOS circuits, there are two sources of power dissipation: the dynamic power used to switch the state of a gate, and the static power used when a gate is at steady-state. In this spin-diode logic family, there is only static power dissipation, and no dynamic power dissipation. This behavior is because the anode and cathode of each spin-diode are always connected, respectively, to V_{DD} and ground, and no charge needs to accumulate to switch a voltage state.

5.2 Comparison to CMOS

While spin-diode logic is in its early stages of development, it shows promise as a potential replacement for CMOS. In particular, spin-diodes have a more compact logic structure and advantageous material properties.

5.2.1 Compact Logic

As implied in section 2, the spin-diode is most effective when implementing inverters, NOR gates, XNOR gates, and OR gates. While other logic functions, such as AND and NAND, can be implemented with a combination of these basis gates, these logic functions require additional gates, resulting in greater area, delay, and power consumption. It is thus worthwhile to consider the implementation of larger logic blocks, as it may frequently be difficult to optimize smaller logical functions. Most logical functions can be implemented with many fewer devices than its Si CMOS counterpart, as each diode has the equivalent functionality of at least two transistors. For example, an adder is here created using only six spin-diodes, which is far more compact than the

typical CMOS 28-transistor implementation. Furthermore, the use of a single device type simplifies the fabrication process. The multiplexer, however, is not easily optimized in this logic family. When a multiplexer is an element of a combinational logic circuit, it should be considered as part of a larger circuit.

5.2.2 Power-Delay Product

An important performance metric of a device is the power-delay product (PDP). The PDP of the current heterojunction diode is

$$PDP = \frac{I_{ON} + I_{OFF}}{2} V_{DD} t_D, \quad (4)$$

where I_{ON} and I_{OFF} are the ‘1’ and ‘0’ currents, respectively. At 0.3 V, preliminary analysis of the switching time of the device exhibits a worst case propagation delay t_D on the order of 10 ns. The PDP is thus approximately 2×10^{-10} J. With scaling, it is expected that this metric will be greatly improved. In particular, if the junction diameter is decreased from 300 nm to 30 nm, the junction area and current will decrease by a factor of 10^8 , and if the length is decreased from 400 nm to 40 nm, the delay will decrease by a factor of 10^4 . A PDP on the order of 10^{-22} J is therefore possible, although other effects are likely to increase the power and delay. As the mobilities in InAs are significantly higher than in Si, these estimates compare favorably with standard Si CMOS technologies, which exhibit a PDP on the order of 10^{-15} J.

6. CONCLUSIONS

This logic family is an effective method for exploiting the InMnAs magnetic semiconductor heterojunction. In its current state of development, the diode characteristics are suitable for this logic family, and the performance characteristics are expected to improve with future work. In particular, by increasing the Mn content of the heterojunction, the diode is predicted to have increased magnetoresistance. Experimentation with dielectrics and other materials will likely also result in a higher B/I ratio. Additionally, as the device is scaled to nanometer dimensions, the delay and power consumption will decrease. In concert with an expanded design space including the use of recently demonstrated InMnAs transistors and the application to memory and reconfigurable logic, this device and accompanying logic family has the potential to replace CMOS and thereby have a significant impact on the future of computing.

7. REFERENCES

- [1] R. H. Chen, A. N. Korotkov, and K. K. Likharev, “Single-electron transistor logic,” *Appl. Phys. Lett.*, vol. 68, pp. 1954-1956, Apr. 1996.
- [2] A. Bachtold, P. Hadley, T. Nakanishi, and C. Dekker, “Logic circuits with carbon nanotube transistors,” *Science*, vol. 294, pp. 1317-1320, Nov. 2001.
- [3] A. Geim and K. Novoselov, “The rise of graphene,” *Nature Materials*, vol. 6, pp. 183-191, Mar. 2007.
- [4] L. Liao *et al.*, “High-speed graphene transistors with a self-aligned nanowire gate,” *Nature*, vol. 467, pp. 305-308, Sep. 2010.
- [5] Y. Huang *et al.*, “Logic gates and computation from assembled nanowire building blocks,” *Science*, vol. 294, pp. 1313-1317, Nov. 2001.
- [6] C. P. Collier *et al.*, “Electronically configurable molecular-based logic gates,” *Science*, vol. 285, pp. 391-394, July 1999.
- [7] S. Datta and B. Das, “Electronic analog of the electro-optic modulator,” *Appl. Phys. Lett.*, vol. 56, pp. 665-667, Feb. 1990.
- [8] H. Akinaga and H. Ohno, “Semiconductor spintronics,” *IEEE Trans. Nanotechnology*, vol. 1, pp. 19-31, Mar. 2002.
- [9] A. Ney, C. Pampuch, R. Koch, and K. H. Ploog, “Programmable computing with a single magnetoresistive element,” *Nature*, vol. 425, pp. 485-487, Oct. 2003.
- [10] D. A. Allwood *et al.*, “Magnetic domain-wall logic,” *Science*, vol. 309, pp. 1688-1692, Sep. 2005.
- [11] A. Imre, G. Csaba, L. Ji, A. Orlov, G. H. Bernstein, and W. Porod, “Majority logic gate for magnetic quantum-dot cellular automata,” *Science*, vol. 311, pp. 205-208, Jan. 2006.
- [12] S. J. May and B. W. Wessels, “High-field magnetoresistance in p-(In,Mn)As/n-InAs heterojunctions,” *Appl. Phys. Lett.*, vol. 88, pp. 072105-1-3, Feb. 2006.
- [13] A. Khitun, M. Bao, and K. L. Wang, “Spin wave magnetic nanofabric: a new approach to spin-based logic circuitry,” *IEEE Trans. Magnetics*, vol. 44, pp. 2141-2152, Sep. 2008.
- [14] N. Rangaraju, P. C. Li, and B. W. Wessels, “Giant magnetoresistance of magnetic semiconductor heterojunctions,” *Phys. Rev. B*, vol. 79, pp. 205209-1-5, May 2009.
- [15] S. Sugahara and J. Nitta, “Spin-transistor electronics: an overview and outlook,” *Proc. IEEE*, vol. 98, pp. 2124-2154, Dec. 2010.
- [16] S. A. Wolf, J. Lu, M. R. Stan, E. Chen, and D. M. Treger, “The promise of nanomagnetism and spintronics for future logic and universal memory,” *Proc. IEEE*, vol. 98, pp. 2155-2168, Dec. 2010.
- [17] J. A. Peters, N. Rangaraju, C. Feeser, and B. W. Wessels, “Spin-dependent magnetotransport in a p-InMnSb/n-InSb magnetic semiconductor heterojunction,” *Appl. Phys. Lett.*, vol. 98, pp. 193506-1-3, May 2011.
- [18] F. M. Wanlass, “Low stand-by power complementary field effect circuitry,” US Patent # 3,356,858, Dec. 1967.
- [19] R. H. Katz, *Contemporary Logic Design*. Redwood City, CA: Benjamin/Cummings, 1994, pp. 669-670.
- [20] J. S. Friedman, N. Rangaraju, Y. I. Ismail, and B. W. Wessels, “A Spin-Diode Logic Family,” *IEEE Trans. Nanotechnology* (in review).
- [21] J. Sklansky, “Conditional-sum addition logic,” *IRE Trans. Electronic Computers*, vol. 9, pp. 226-231, Jun. 1960.
- [22] B. W. Wessels, “Ferromagnetic semiconductors and the role of disorder,” *New J. Phys.*, vol. 10, pp. 055008-1-17, May 2008.