Abstract—Current through ambipolar carbon nanotube field-effect transistors (CNTFETs) can be controlled by two independent gates, enabling highly expressive XOR-based logic circuits. To promote efficient circuit design, it is important to develop an easy-to-use SPICE-compatible model for these dual-gate ambipolar CNTFETs. This paper therefore introduces a closed-form model that matches the experimentally demonstrated behavior. This model is then applied for the first simulation of cascaded dual-gate CNTFET logic circuits that exploit ambipolarity for compact logic.

Keywords—carbon nanotube transistor, ambipolar transport, dual independent gates, device model, emerging technologies.

I. INTRODUCTION & BACKGROUND

Carbon nanotube field-effect transistors (CNTFETs) have been widely investigated as potential replacements for CMOS as scaling approaches its fundamental physical limitations [1]. Their exceptionally high current density coupled with their tunable bandgap enables improved transistor behavior, while their small size and one-dimensional transport are attractive from a scaling perspective. Additionally, the CNT ambipolarity permits the continuous conversion of a single CNTFET between primarily electron or hole transport [2]–[4].

This ability to switch between $n$-FET and $p$-FET operation has inspired investigation into new avenues for logic circuit design with ambipolar CNTFETs controlled by two independently-biased gates. The most popular approach considers pairs of such dual-gate ambipolar CNTFETs in complementarily-addressed pull-up and pull-down structures [5]. This static binary logic provides a four-device full-swing XOR gate, enabling the compact design of a wide range of logic functions [5]. Alternatively, dual-gate ambipolar CNTFETs have been integrated into a static multiplexer-based design style [6], as well as in clocked dynamic logic [7]. The XOR-based structure is particularly promising, leading to its implementation with ambipolar silicon nanowires [8], [9].

The further development of compact logic circuits based on dual-gate ambipolar CNTFETs is impeded by the absence of a straightforward SPICE-compatible device model that enables manipulation of both independent gate voltages. In particular, the early work in this field considered the ambipolar CNTFET as a conventional MOSFET with current modulated by a single “control gate” [5], [6], [10]. In that model, a “polarity gate” was considered solely as a binary state that determined whether the CNTFET acted as an $n$-FET or $p$-FET; modulation of the “polarity gate” voltage was not considered. An extremely thorough model was developed in [11], but its utility is severely diminished by its complexity and abundance of parameters.

This challenge extends to ambipolar silicon nanowire models, which are largely based on physical simulation tools that do not facilitate circuit analysis with multiple devices [8], [9], [12].

In this paper, we develop a closed-form model that supports the design and analysis of dual-gate ambipolar CNTFET circuits. This model is validated through comparison to the available experimental data [2], [4], permitting the first SPICE simulation of cascaded dual-gate CNTFET logic circuits that exploit the ambipolarity. These simulation results are then analyzed to provide guidance for ambipolar CNTFET circuit design.

II. DUAL-GATE AMBIPOLAR CNTFET MODEL

This SPICE-compatible model determines the source-drain current $I_D$ through consideration of the CNTFET source, drain, bottom gate, and top gate voltages. Unlike previous work, this model considers the bottom gate voltage as a variable rather than simply as the selector of the CNTFET polarity.

A. Structure & Physical Behavior

The dual-gate ambipolar CNTFET is shown in Fig. 1 with a CNT channel connected between source and drain contacts. Independent voltages on the top and bottom gates are capacitively coupled to the CNT channel through $C_{TG}$ and $C_{BG}$, controlling the quantity and polarity of charge carriers. The source-drain current is thus modulated by all four node voltages. The top gate functions similarly to a conventional MOSFET gate, with the electric potential between the top gate and source ($V_{TG,S}$) controlling the charge carrier density within the CNTFET channel. When sufficient electric potential is applied to the top gate and across $C_{TG}$, the CNTFET threshold voltage $V_{TH,TG}$ is overcome and charge carriers are excited within the CNTFET. These excited charges are then free to flow between the source and drain.

The bottom gate provides an additional means of controlling the source-drain current. The application of an electric potential between the bottom gate and the source ($V_{BG,S}$) modifies the charge carrier density throughout the CNTFET. The region of operation is then determined by the interplay of the top and bottom gate voltages.

![Fig. 1. Cross-sectional diagram of dual-gate ambipolar CNTFET (adapted from [2]).](image-url)
When the two gate voltages are equal, the energy bands are structured as shown in Fig. 2. For equal positive \( V_{TG,S} \) and \( V_{BG,S} \) respectively greater than threshold voltages \( V_{TH,TG} \) and \( V_{TH,BG} \), the conductance and valence bands are lowered, enabling electrons to travel from the source to the drain. If the \( V_{TG,S} \) and \( V_{BG,S} \) have similar negative values below \( V_{TH,TG} \) and \( V_{TH,BG} \), the raised valence band level allows holes to move through the CNT from source to drain, as in Fig. 2(b).

When different voltages are applied to the two independent gates, the interactions are more complex. As can be seen in Fig. 3, the relative voltages of the two gates determines the height of the energy barrier faced by electrons and holes when traveling between regions A and B. When the voltages are properly matched, the energy barrier can be minimized to enable charge flow between the source and drain; alternatively, the gate voltages can be set to impede current flow. Control of the energy barrier thus governs charge flow in the channel.

The two highly conductive states are reached by applying gate-source voltages of similar polarity to the two independent gates. When a positive \( V_{BG,S} \) is applied as in Fig. 3(a), the energy bands are lowered. If \( V_{TG,S} \) is also positive, the energy bands in region B follow the solid line. This flattened band at the boundary between regions A and B permits electrons to travel through the CNT channel. The CNTFET thus functions similarly to an n-FET with a conducting channel, which can be considered the “ON” state. Similarly, the application of negative \( V_{BG,S} \) and \( V_{TG,S} \) results in the dashed higher energy flattened bands of Fig. 3(b), enabling hole transport through the CNT channel. Here, the CNTFET functions as a conducting p-FET in an “ON” state.

When the two gate voltages are of opposite polarity, a large barrier between the energy bands in regions A and B impedes current flow through the CNT channel. In the presence of positive \( V_{BG,S} \) and negative \( V_{TG,S} \), the raised (dashed line of Fig. 3(a)) energy bands in region B prevent electrons from entering region B from region A. Similarly, a negative \( V_{BG,S} \) and positive \( V_{TG,S} \) causes lowered (solid line of Fig. 3(b)) band energies in region B, preventing holes from entering region B from region A. In both of these cases, the top gate acts as a barrier impeding the flow of charge carriers through the CNT channel. The CNTFET can thus be considered in an “OFF” state. This dual control of the CNTFET state provides added expressive power and permits compact CNTFET circuits.

### B. Calculation of Source-Drain Current

To enable circuit design with dual-gate ambipolar CNTFETs, a closed-form model is developed [13] to calculate the drain-source current as a function of all four independent node voltages. As minimal experimental data is available, this model has been developed to match the highly conductive CNTFET states most relevant to logic circuit design; the highly resistive states are not well-described by this model.

To determine the charge carrier density, \( V_{TG,S} \) can be written as a function of the top gate-to-channel voltage \( V_{TG,C} \) and the channel-to-source voltage \( V_{C,S} \):\[
V_{TG,S} = V_{TG,C} + V_{C,S}.
\] (1)

An effective channel-to-source voltage \( V_{C,S,eff}(x) \) can be defined to characterize the amount by which the voltage exceeds \( V_{TH,TG} \) at various points \( x \) along the CNT channel, enabling (1) to be rewritten as\[
V_{TG,C} = V_{TG,S} - V_{TH,TG} - V_{C,S,eff}(x).
\] (2)

The threshold voltages are defined separately for the \( n \)- and \( p \)-type CNTFET regimes. The charge carrier density \( Q(x) \) can then be calculated as a function of the top gate capacitance \( C_{TG} \):\[
Q(x) = C_{TG} (V_{TG,C} - V_{TH,TG} - V_{C,S,eff}(x)).
\] (3)

The current resulting from the top gate control of the charge density is determined by the electric field \( E \) in the CNT channel, \( E = \frac{\partial V_{C,S}}{\partial x} \). The drain-source current \( I_{DS,TG} \) resulting from the top gate can then be written as\[
I_{DS,TG} = \frac{\mu W Q(x) E}{x} = \frac{\mu W Q(x) \partial V_{C,S}}{\partial x},
\] (4)

where \( \mu \) is the conductivity of carriers and \( W \) the CNTFET width. Integrating from source voltage \( V_S \) to drain voltage \( V_D \) along the length \( L \) of the CNT channel gives\[
I_{DS,TG} = \frac{\mu W C_{TG}}{L} \left[ (V_{TG,S} - V_{TH,TG}) V_{DS} - \frac{V_{DS}^2}{2} \right].
\] (5)

To determine the saturation voltage \( V_{DS,TG,SAT} \) can be evaluated and set to 0:
\[
\frac{\partial I_{DS}}{\partial V_{DS}} = (V_{TG,S} - V_{TH,TG}) - V_{DS} = 0 \quad (7)
\]
\[
V_{DS,TG,SAT} = V_{TG,S} - V_{TH,TG}.
\] (8)

The saturation current \( I_{DS,TG,SAT} \) resulting from the top gate voltage can then be calculated as\[
I_{DS,TG,SAT} = \frac{\mu W C_{TG}}{2L} (V_{TG,S} - V_{TH,TG})^2.
\] (9)

The bottom gate has an analogous interaction with the source-drain current. A similar derivation can be performed by replacing \( C_{TG} \) with \( C_{BG} \), \( V_{TG,S} \) with \( V_{BG,S} \), and \( V_{TH,TG} \) with bottom gate threshold \( V_{TH,BG} \). The source-drain current \( I_{DS,BG} \) resulting from carriers excited by the bottom gate voltage is...
\[ I_{DS,BG} = \frac{\mu_{TBG} C_{BG}}{L} \left[(V_{BG-S} - V_{TH,BG})V_{DS} - \frac{V_{DS}^2}{2}\right]. \] (10)

leading to a saturation current \( I_{DS,BG,SAT} \) due to the bottom gate
\[ I_{DS,BG,SAT} = \frac{\mu_{TBG} C_{BG}}{2L} (V_{BG-S} - V_{TH,BG})^2. \] (11)

The available experimental data (but not the precise underlying physical mechanisms) can be approximated. By combining the top and bottom gate square-law current contributions to produce a total source-drain saturation current \( I_{DS,SAT} \) given by
\[ I_{DS,SAT} = \kappa (V_{TG-S} - V_{TH,TG})^2 (V_{BG-S} - V_{TH,BG})^2, \] (12)

where \( \kappa \) is a fitting parameter related to the mobility, capacitances, and size of the CNTFET components.

### III. EXPERIMENTAL VALIDATION

The model defined in section II matches well the experimental data from Lin et al. [2]. As limited physical analysis is available for dual independent-gate ambipolar CNTFETs, \( \kappa \), \( V_{TH,TG} \), and \( V_{TH,BG} \) are extracted from the experimental data to reproduce the CNTFET behavior. By evaluating the device under the same ON-state conditions tested experimentally, the model is shown to correspond to the physical device in the highly conductive states.

Fig. 4 shows the analysis of the CNTFET under the same conditions described by the energy band diagrams of Fig. 2. In this case, \( V_{TG,S} \) and \( V_{BG,S} \) are equivalent and are swept from -2V to +2V with \( V_{DS} = -0.6 \) V. As can be seen in Fig. 4, the model is consistent with the experimental data (Fig. 4(a) of [2]). In both the ON\(_n\) \( (V_{TG,S} = V_{BG,S} > V_{TH}) \) and ON\(_p\) \( (V_{TG,S} = V_{BG,S} < V_{TH}) \) states, the ambipolar source-drain current is seen to rise quickly with voltages of increasing magnitude. When the gate voltage is between the \( V_{TH,n} \) and \( V_{TH,p} \), the CNTFET conducts a negligible “OFF” current below the scale of the figure.

The more complex case of separately-addressed independent gate voltages is evaluated in Fig. 5. These conditions, described physically by Fig. 3, are characterized by sweeping \( V_{TG,S} \) from -2V to +2V for two static \( V_{BG,S} \) values (-2V and +1.6V). The results derived from the model are consistent with the experimental data (Fig. 6 of [2]). As in the previous experiment, the distinct ON\(_n\) and ON\(_p\) states can be observed, with negligible source-drain current when either or both of the gate voltages are below threshold.

### IV. CASCADED COMPACT CIRCUIT DESIGN WITH DUAL-GATE AMBIPOLAR CNTFET MODEL

This model is sufficient for the preliminary design of compact logic circuits based on dual-gate ambipolar CNTFETs. To demonstrate the utility of the model, single and cascaded XOR gates are simulated and analyzed to explore circuit design challenges with dual-gate ambipolar CNTFETs. While there has been much analysis of individual ambipolar logic gates, this is the first analysis of cascaded dual-gate ambipolar CNTFET logic gates that exploit the ambipolarity.

#### A. Four-CNTFET XOR Gate

Fig. 6 depicts two cascaded XOR logic gates composed of ambipolar dual-gate CNTFETs based on the single-XOR structure of [5]. Each XOR gate is composed of four CNTFETs such that either the pull-up or pull-down networks are conductive, leading to a voltage on output node \( X \) of either \( V^+ \) or \( V^- \), respectively. When both inputs \( A \) and \( B \) have the same polarity, both pull-down CNTFETs (T3 and T4) in the leftmost XOR gate are in ON states and both pull-up CNTFETs are in OFF states. For \( A = B = 1 \), T3 is in the ON\(_n\) state and T4 is in the ON\(_p\) state; when both inputs are ‘0’, T3 is in the ON\(_p\) state and T4 is in the ON\(_n\) state. In both cases, there is no threshold drop across the CNTFET in the ON\(_n\) state, leading to an output voltage of \( V^- \). Similarly, when \( A \neq B \), T1 and T2 are in ON\(_n\) and ON\(_p\) states, and the output is \( V^+ \).

The complexities of the circuit design are evaluated in Fig. 7, in which the black line illustrates the ratio of the output of a single XOR gate relative to the supply (and input) voltages. When \( V^+ = V^- = 0 \), \( V_{TG,S} = V_{BG,S} > V_{TH} \), and all CNTFETs are in the \( n\)-FET state. As the supply (and input) voltages are
increased for the case of $A = B = 0$ (Fig. 7(a)), $T_4$ becomes dominant in the ON state and provides a short circuit between $X$ and $V$. The ‘0’ output response is similar for $A = B = 1$, with $T_4$ replaced by $T_3$.

When $A = 0$ and $B = 1$ (Fig. 7(b)), $V_{BG-S}$ is 0 for both $T_2$ and $T_4$, causing $T_1$ to enter the ON $p$ region as the input and supply voltages are increased for the case of $A = 1$ and $B = 0$. The asymmetries found in Fig. 7 are a result of the asymmetric thresholds in the experimental data [2], with the transistors’ initial ON $n$ states leading to a higher transition current when $X = 1$. By achieving greater balance in threshold voltages, the switching speed and power consumption of this CNTFET circuit can be further enhanced.

**B. Cascaded CNTFET XOR Gates**

The two circuits in Fig. 6 function as two cascaded XOR gates, differentiated by their cascading configurations. In both configurations, the circuits perform the function

$$Y = X \oplus C = A \oplus B \oplus C. \quad (13)$$

In Fig. 6(a), the output of the first XOR is connected to top gates in the second XOR; in Fig. 6(b), the first XOR output is connected to bottom gates in the second XOR.

The simulated output ratios for both configurations are presented in the blue and red lines of Fig. 7 for all input combinations. As can be seen in the plots, the output voltage $Y$ switches sharply whenever a pull-up CNTFET switches into the ON $n$ region. In both cases, this transition occurs near the $V_{TH(p)}$ value determined from [2]. This sharp switching effect is less pronounced for the pull-down CNTFETs in the ON $p$ state due to their lower threshold voltages.

It can be observed from the plots that when the output signal is connected to the top gate of the next stage, the cascaded XOR gates provide a superior $V_{out}^{\text{XOR}} / V^{+}$ ratio. Furthermore, the top gate cascading produces rail-to-rail voltage swing with a smaller supply voltage. In both cases, the circuit structure is shown to maintain signal integrity as data flows through the logic circuit. The ability to cascade these full-swing XOR gates therefore inspires further work toward the development of compact circuits based on dual-gate ambipolar CNTFETs.

**V. CONCLUSIONS**

To enable compact logic circuit design based on dual-gate ambipolar CNTFETs, a closed-form SPICE-compatible model has been developed. Unlike previous models that use one gate voltage only to set the polarity, this model permits control of the current through modulation of both independent gate voltages. This model is verified to accurately reproduce the published experimental data, and its utility for cascaded circuit design is demonstrated. By enhancing the circuit design flow of these highly expressive dual-gate ambipolar CNTFETs, this work provides a significant advance toward the design of compact XOR-based CNTFET logic circuits.

**ACKNOWLEDGMENTS**

The authors thank M. C. Hersam, M. L. Geier, A. V. Sahakian, S. Frégonèse, and P.-E. Gaillardon for helpful conversations and input.

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