Sequential Circuit Design with Bilayer Avalanche Spin Diode Logic

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ABSTRACT

Novel computing paradigms like the fully cascadable InSb bilayer avalanche spin-diode logic (BASDL) are capable of performing complex logic operations. Although the original work provides a comprehensive explanation for the device structure, the fundamental logic set and basic combinational circuits, it lacks the inclusion of sequential circuit design. This paper addresses the void by demonstrating the structural design of SR and D-type latches with BASDL. Novel latch topologies are proposed that take full advantage of the BASDL-based logic set while maintaining conventional latch functionality. The effective operation of these latches is verified through a complete logic-level analysis and a brief insight into their physical implementation.

CCS CONCEPTS

• **Hardware → Spintronics and magnetic technologies**;

KEYWORDS

Spin-Diodes, Flip-Flops, Spintronics

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1 INTRODUCTION

Emerging device technologies like spintronics promisingly serve as the foundation for the next generation of computing paradigms [1–6]. Ref. [4] improves on the proposal by Joo *et al.* [3] by devising a fully cascadable bilayer avalanche spin-diode logic (BASDL) structure. On one hand, the efficient cascading scheme enables the design of more compact circuits, while on the other, faster switching speeds are attainable due to their dependence on electromagnetic wave propagation delay rather than *RLC* delay [4, 6].

Both combinational and sequential circuits are required in a computing system. As opposed to combinational logic circuits whose state depends on the instantaneous values of the inputs, sequential logic circuits involve a 'memory element' that enables response to both the present and previous input states. The simplest form of a sequential circuit is a latch designed using a set of cross-coupled inverters capable of holding a single bit of information. The set-reset (SR) latch and the D latch are more commonly used and are usually structured using cross-coupled NAND or NOR gates.

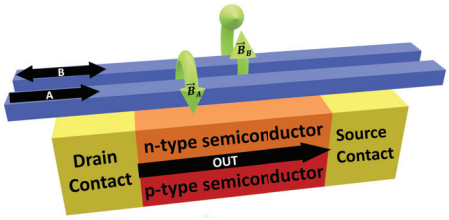

Figure 1: Bilayer avalanche spin-diode, where the magnetic fields due to input currents A and B modulate the output current.

Although Ref. [4] details basic combinational circuit design with BASDL, it fails to include any description about its use in sequential circuits. This paper proposes the design of SR and D latches using the BASDL logic family. Section 2 details the BASDL device from a structural and logic-implementation perspective. Sections 3 and 4 describe two latch topologies each for the SR and D latch respectively: conventional cross-coupled gates, followed by a novel topology that fully exploits the basis logic set provided by BASDL.

2 BILAYER AVALANCHE SPIN-DIODE LOGIC

A spin-diode is a device with a negative magnetoresistance whose resistance state (and hence the output current) is modulated by the application of an external magnetic field. In the case of BASDL, this magnetic field is a result of the additive and counteractive interaction between the individual magnetic fields created by two current carrying wires A and B (Fig. 1) [4]. The magnitude and direction of the resultant magnetic field with respect to a threshold determine the resistance state of the spin-diode. Here, a logic '1' is a large current, whereas a small current is the equivalent of logic '0'.

Since the output currents can be used to feed the control wires of subsequent BASDL devices, this scheme allows for a fully cascadable design without the use of any amplification or control overhead. Further, depending on the relative direction of the two currents, the device performs either an inverted-input AND (IAND = $A \wedge \overline{B}$) or the conventional OR ($A \vee B$) operation, Together, these operations form a complete basis logic set.

3 BASDL SR LATCH DESIGN

The most fundamental latch constructed using basic CMOS logic gates is the 'set-reset' (SR) latch. IAND gates can be used to devise

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Table 1: Truth table for cross-coupled IAND SR Latch

Characteristic Table				Excitation Table			
S	R	Q_{next}	State	Q	Q_{next}	S	R
0	0	X	Forbidden	0	0	0	X
0	1	0	Reset	0	1	1	0
1	0	1	Set	1	0	0	1
1	1	Q	Hold	1	1	X	0

a similar latch using the cross-coupled topology of the SR NOR and NAND latches (Fig. 2a). As shown in Table 1, the output Q is 'set' when $S = 1$ and $R = 0$, and 'reset' when $S = 0$ and $R = 1$. Further, if $S = 1$ and $R = 1$, the latch retains its previous state (hold state), whereas at $S = 0$ and $R = 0$, the output cannot be determined with certainty (forbidden state). Therefore, the characteristic equation of the cross-coupled IAND-OR logic can be written as

$$Q_{next} = S\overline{R} + QR, \tag{1}$$

where Q and Q_{next} are the present and next states of the latch, respectively. It can be noted that the hold and forbidden states are interchanged relative to a conventional CMOS SR latch.

An alternate, yet simpler structure consists of a cross-coupled IAND-OR loop (Fig. 2b) and behaves as a regular SR latch having the characteristic equation given by (2); the standard truth table is not shown here. This structure is particular to the basis logic set provided by BASDL, and is described by (2). Fig. 3 shows the physical implementation of the cross-coupled IAND-OR SR latch [4].

$$Q_{next} = S\overline{R} + Q\overline{R}. \tag{2}$$

4 BASDL D LATCH DESIGN

The forbidden state of the SR latch can be eliminated by disallowing simultaneous identical inputs such that the reset input is replaced by $\overline{D}$ as the complement of set input D. A gated D latch with an active-low enable signal (En) can be designed using either of the two SR latch structures described in the previous section (Fig. 4). Fig. 4a shows a D latch constructed using the cross-coupled IAND SR latch. An IAND gate with a fixed high non-inverted input acts as an inverter and prevents the latch from entering the forbidden state. When the enable signal is low, the latch is set or reset in accordance with the D input; otherwise the latch retains its previous state (Table 2). Hence, the characteristic equation of this latch is given by (3):

$$Q_{next} = \begin{cases} Q, & \text{when } En = 0 \\ D, & \text{when } En = 1. \end{cases} \tag{3}$$

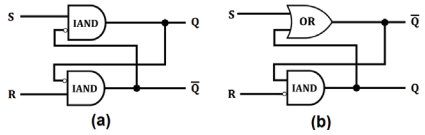

Figure 2: Schematic for an SR latch with (a) cross-coupled IAND gates and (b) cross-coupled IAND-OR loop.

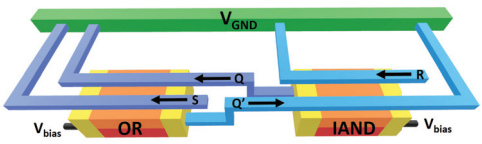

Figure 3: Physical implementation of a cross-coupled IAND-OR SR latch.

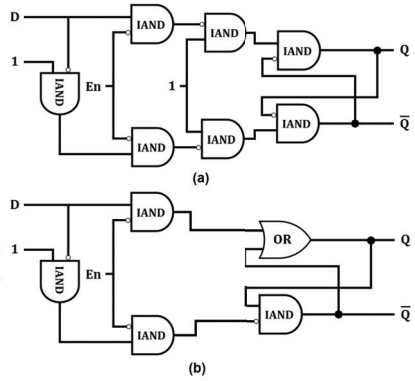

Figure 4: Schematic for a D Latch with (a) cross-coupled IAND SR latch and (b) cross-coupled IAND-OR SR latch.

Table 2: Truth table for cross-coupled IAND D Latch

Characteristic Table				Excitation Table		
En	D	Q_{next}	State	Q	Q_{next}	D
0	0	Q	Hold	0	0	0
0	1	Q	Hold	0	1	1
1	0	0	Reset	1	0	0
1	1	1	Set	1	1	1

The above structure requires the use of additional IAND gates as inverters prior to the SR latch stage for proper latch operation. This extra inversion stage can be eliminated by exploiting the cross-coupled IAND-OR SR latch described in the previous section. The characteristic equation and truth table of the resultant structure (Fig. 4b) is identical to a conventional D latch and is not shown here. This results in a significant reduction in the gate count and total gate delay, in concert with the lower switching times of bilayer avalanche spin-diodes [6].

5 CONCLUSIONS

The fully cascadable design and faster switching speeds enable BASDL to provide for a promising pathway towards efficient alternatives to conventional computing methods. This paper describes the design of fundamental latch topologies tailored to the BASDL logic set, making sequential computing possible for the first time. The proposed design can be extended, with relative ease, to other computing methods with asymmetric logic operations (similar to IANDs) as part of their fundamental logic set.

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