EE 6302: Microprocessor Systems
(Fall 2000, Tuesday and Thursday: 5:30–6:45 p.m., MP 3.226)

1 General Information

Instructor: Mehrdad Nourani
Office & Phone: EC 3.522, 972-883-4391
E-mail: nourani@utdallas.edu
Office Hours: Tuesday and Thursday 2:30–3:30 p.m., or by appointment.
References: Related papers from literature.
2. Co-Synthesis of Hardware and Software for Digital Embedded Systems, R. Gupta,
3. The 8051 Microcontroller and Embedded Systems, Muhammad A. Mazidi and
Course Web Page: http://www.utdallas.edu/~nourani/Teaching/fa00_ee6302/
Teaching Assistant: To be announced.

2 Catalog Description

EE 6302: Microprocessor Systems (3 semester hours).
Design of microprocessor based systems including I/O and interface devices. Microprocessor architectures. Use of
emulators and other sophisticated test equipment. extensive laboratory work.
Prerequisite: Digital design (e.g. EE 4320 or equivalent).
Basic background on computer architecture.

3 Grading

Grading will be based on step-by-step implementation of a microprocessor-based system project.

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\begin{align*}
\text{Phase 1: Market survey and analysis} & \quad 15\% \ (\text{Tue. 9-12-2000}) \\
\text{Phase 2: Design specifications and feasibility study} & \quad 15\% \ (\text{Tue. 9-26-2000}) \\
\text{Phase 3: Instruction set and system/RT level design} & \quad 25\% \ (\text{Tue. 10-17-2000}) \\
\text{Phase 4: Progress report on simulation and implementation} & \quad 25\% \ (\text{Tue. 11-7-2000}) \\
\text{Phase 5: Final report and presentation} & \quad 20\% \ (\text{Tue. 11-28 and Thur. 11-30-2000})
\end{align*}
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4 Course Policy

- Objective: The objective of this course is to introduce and expose students to methodologies for systematic
design of processors and processor-based embedded systems. It is expected that the student will acquire a clear
understanding of both the hardware and software techniques and strategies for developing a new processor or
a processor-based embedded system.

- Projects: You can work on the project individually or in a group of two. A network processor (also called
Network Instruction Set Computer or NISC) will be studied, designed and partially implemented. The ration-
ale, applications, market demand and specification of such processor for networking tasks will be studied
first (Phase 1 and 2). Then, based on the common tasks needed for IP packet processing an instruction set
and system/RT level structure will be proposed to achieve certain speed and capabilities (Phase 3). Finally, it
is expected that the processor, completely designed in Phase 3, to be implemented at least partially (e.g. the
CPU core, the serial IO interface, etc.) to show the correctness of design and fundamental approach (Phase 4).
The students have different backgrounds, experience levels and familiarity with design tools. Therefore, for the implementation (Phase 4), they are allowed to use CAD synthesis/simulation tools, hardware description language and/or hardware development environments (such as the 8051 development boards) of their choice.

- **Laboratory:** The Embedded System Laboratory (EC 3.120) will be available to the students to help them with their hardware implementation. Some key lab equipments such as PC hosts with some general-purpose softwares, oscilloscope, logic analyzer, function generator, power supply, PROM programmer and eraser, etc. will be available during the lab hours (to be announced in the web page). Sample 8051 boards are also available in the lab and you are welcome to use them. However, due to the learning curve and the need to keep the assembled components of your project for further development, having your own board is strongly recommended. As for CAD tools, at present SYNOPSYS, CADENCE and TI-SPICE are available on almost all Unix machines in EC building such as Solarium Lab.

- **Report/Demo:** You need to prepare your technical reports at the end of each phase in a professional way. These documents should show clearly your work and investigation/design process. If necessary you need to make arrangements for demo before or on the due dates. Late or make-up reports, demos or presentations will not be accepted unless the student has obtained permission from the instructor before the due date. Permission will not be given without documentation of exceptional circumstances.

- **Attendance:** Regular attendance is highly recommended. Announcements and complementary materials will be posted on the course web page.

### 5 Syllabus & Tentative Lecture Plan

<table>
<thead>
<tr>
<th>Weeks</th>
<th>Readings</th>
<th>Topics Coverage</th>
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<tbody>
<tr>
<td></td>
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<td><strong>Topics Coverage</strong></td>
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<tr>
<td>Tue.</td>
<td>Thur.</td>
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<tr>
<td>8/24</td>
<td>An Arch. book</td>
<td><strong>Introduction:</strong> course introduction; technologies and style; y-chart; current CAD design methodologies.</td>
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<tr>
<td>8/29</td>
<td>8/31</td>
<td><strong>Microprocessor Systems:</strong> Data path and controller path microarchitectures; application specific processors; RISC and CISC;</td>
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<tr>
<td>9/5</td>
<td>9/7</td>
<td>Papers</td>
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<tr>
<td>9/12</td>
<td>9/14</td>
<td><strong>Network Processors:</strong> applications; market demand;</td>
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<tr>
<td>9/19</td>
<td>9/21</td>
<td>Internet</td>
</tr>
<tr>
<td>9/26</td>
<td>9/28</td>
<td>Hardware Description Languages: modeling; concurrency; hierarchy; timing.</td>
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<tr>
<td>10/3</td>
<td>10/5</td>
<td>Papers</td>
</tr>
<tr>
<td>10/10</td>
<td>10/12</td>
<td><strong>The 8051 Microcontroller:</strong> architecture; assembly language; I/O port access; jumps and loops; procedure calls;</td>
</tr>
<tr>
<td>10/17</td>
<td>10/19</td>
<td>An 8051 book</td>
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<tr>
<td>10/24</td>
<td>10/26</td>
<td>arithmetic and logic instructions; timer/counter programming and interfacing; interrupts.</td>
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<tr>
<td>10/31</td>
<td>11/2</td>
<td>An 8051 book</td>
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<tr>
<td>11/7</td>
<td>11/9</td>
<td>interrupts priority and programming. strobing versus handshaking; serial communication;</td>
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<td>11/14</td>
<td>11/16</td>
<td>Ref. 1, Papers</td>
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<tr>
<td>11/21</td>
<td>11/23</td>
<td><strong>Partitioning:</strong> granularity; metrics; estimation algorithms; clustering algorithm; functional partitioning.</td>
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**Final demo, presentation and report.**