

Venkatesh Acharya

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SUMMARY

A highly qualified, self motivated electrical engineer with specialization in analog integrated circuit design. A thorough knowledge in **Analog filters, Delta-Sigma modulator, Flash converters** design and characterization. As a dedicated team player, works towards better product and with maximum efficiency. Seeking a challenging **analog/mixed-signal/RF IC design** position in the best company which encourages self development by support for learning new knowledge in the field of state of art analog/mixed-signal/RFIC Design.

EDUCATION

PhD Candidate, Department of Electrical Engineering Aug 2005 -
University of Texas at Dallas, Richardson TX, GPA 4.0/4.0

Related Research Topics: Low voltage, Low Power, High speed Data Converters, Analog Active Filters, RF Circuits.

Adviser: Prof. TR Viswanathan, Professor, University of Texas at Austin.

Master of Technology, Electrical Engineering 2002 – 2004
Indian Institute of Technology Madras, Chennai, GPA 3.6/4.0

Dissertation: Design and Implementation of CODEC for Audio Signal Applications.

Adviser: Dr. Vinita Vasudevan, Assistant professor, IITM

Bachelor of Engineering, Electrical and Electronics Engineering, 1998 – 2002

National Institute of Technology Karnataka, Surathkal, formerly Karnataka Regional Engineering College, Surathkal **GPA 4.0/4.0**

EXPERIENCE

Texas Instruments, Dallas Texas, May 2007 - Dec 2007
Co-op, High Performance Analog Division

24 Bit, 125 Kbps Multibit Low-power Delta-Sigma Modulator

Project involved designing major blocks of a 3rd order feed-forward type modulator including detailed modeling in simulink. Blocks include sampling network, clock generator, integrators, multi-bit quantizer, Digital element matching block and necessary biasing current generation blocks.

24 Bit, 1.024Kbps Ultra low-power Multibit Delta-Sigma Modulator

This project involved designing a 4-bit Flash ADC used in the modulator. Design also included bias-current generators and temperature sensor blocks.

Silicon Laboratories, Austin Texas,
Intern, Analog Group in CAD Division

Aug 2006 - Dec 2006

Validation of 65 nm and 110 nm Process

The project involved validation of schematic and layout cell of all instances in the mentioned process.

Delta Sigma modulator design

This project involved design validation of 65nm and 110nm process. For the undertaken purpose the third order delta sigma modulator for video applications was implemented.

Sanyo LSI Technology Pvt India Ltd, Bangalore, India,
Design Engineer, Analog Group

May 2004 - July 2005

Analog Multiplier

Gilbert-cell based design using 0.18 μ TSMC Process for Wattmeter Applications

Ring Oscillator

10 Mhz Ring oscillator is designed using replica biased differential delay element with 0.18 μ TSMC Process. This design is based on work by Process and temperature compensated CMOS voltage-controlled oscillator for clock generators by Lee S S, Kin S W. This design has been tested successfully on silicon.

Bandgap reference

Curvature compensated Bandgap reference using 0.6 μ Sanyo Process. This design is designed using all BJTs.

Class AB Power Amplifier

250 mW class AB Power Amplifier is designed using 0.15 μ GSMC Process. This design is based on "Large-Swing CMOS Buffer Amplifier" by K Nagaraj. This design has been tested successfully on silicon.

Class D Power Amplifier

Class D Power Amplifier capable of delivering 600mW is designed using 0.15 μ GSMC Process. This design is under fabrication.

TEACHING EXPERIENCE

University of Texas at Dallas, Texas

Aug 2005 - Date

Teaching Assistant. Department of Electrical Engineering

Courses include Advance Analog Circuits, Advanced Analog IC Design, Advanced Analog System Design, RF Integrated Circuit Design, RF and Microwave Communication Circuits and Instrumentation Lab.

Indian Institute of Technology Madras, Chennai India

July 2002 - May 2005

Teaching Assistant. School of Electrical Engineering

Courses include Electrical Circuits, Analog and Digital Circuits Lab, Instrumentation Lab

PUBLICATIONS

1. Acharya Venkatesh "*Design of Class-AB Amplifiers*" Report submitted at Sanyo LSI Technology Pvt India Ltd, Bangalore, India.
2. Acharya Venkatesh, Kakde Sandip, Tantry Shashishar "*Design and Implementation of Class AB CMOS Power Amplifier using 0.15 μ m GSMC Process*" 9th IEEE VLSI Design and Test Symposium 2005.
3. Acharya Venkatesh, T.L. Viswanathan, T.R. Viswanathan "*CMOS Latch Using Quad for High Speed Comparators*" (Accepted for publication in TCAS II)
4. Acharya Venkatesh, "*Quad and its Applications*" Report submitted at UTD.
5. Acharya Venkatesh, T.L. Viswanathan, T.R. Viswanathan "*A Linearized CMOS Quad*" (To be communicated soon)
6. Acharya Venkatesh, T.R. Viswanathan "*A highly linear resistor using series connected Quad*" (To be communicated soon)

COURSEWORK

Analog IC Design, VLSI Design, RFIC Design, Active/Passive Filter Design, VLSI Data Converters and Noise in Electronic Circuits.

Digital Integrated Circuit Design, Design automation of VLSI Systems, Signal Processing and Computer Architecture.

Semiconductor Device Modelling, Advanced MOS Device Modelling, Compound Semiconductors, Power Semiconductors.

Advanced Digital Logic, Advanced Analog System Design, Power Management Circuits.

SPECIAL MENTION

Passed with Distinction in JLPT (Japanese Language Proficiency Test) Level4 in Dec 2004.

REFERENCES

1. Prof. T R Viswanathan tr.viswanathan@utdallas.edu
Professor, University Of Texas Austin
2. Dr. Jim Hellums hellums@utdallas.edu
Fellow, Texas Instruments, Dallas
3. Dr. Shanthi Pavan shanthi@ee.iitm.ac.in
Assistant Professor, Indian Institute of Technology, Madras India