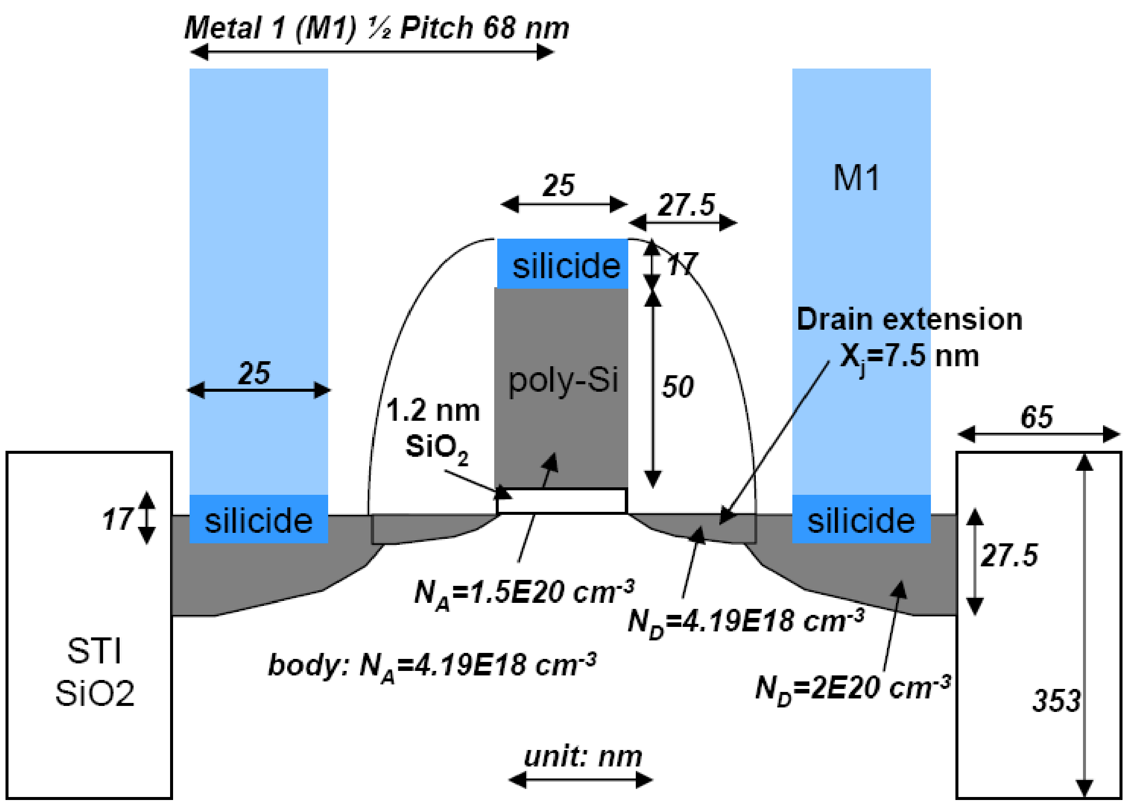
SOLUTION FOR HOMEWORK 2

DESIGN NMOS OF 2007



Considerations for device design:

1. poly-Si is used as gate for ease of fabrication, matched working function, doping was chose to be 1.5E20cm-3 for good conductivity.
2. silicide is formed on poly-Si gate and also source and drain to reduce contact resistance for less signal delays, less power consumption, less heat generation.
3. 1.2 nm SiO2 is used for gate dielectric scaling, well known process but larger gate leakage current compared to high-K dielectric materials. (Option: if use high-K such as HfO2 as gate dielectric layer, advantage is improved gate leakage current)
4. 27.5 nm wide, 7.5 nm deep drain extension lighted doped area is used to improve channel breakdown voltage.
5. The dimensions for all parts are picked from the ITRS roadmap front-end process, P15-16, for year 2007. The reason is for scaling to 65 nm process node.

Device performance prediction:

1. Supply voltage V_{dd}=1.0V, estimated from slide 15, Lecture 2, or ITRS PIDS roadmap.
2. V_t= 0.3 volts, estimated from scaling theory (V_t=0.7V for 3V NMOS).

3. Drive current I_d=1.5 mA/μm, estimated from slide 15, Lecture 2. or can be calculated from equation given in class.
4. junction leakage current: $I_{d,leak}$=0.2 μA/μm, estimated from ITRS roadmap
5. $I_{on}/I_{off} = I_d / I_{d,leak} = 7.5 \times 10^3$
6. gate dielectric leakage current: $J_g = 8\times10^2 A/cm^2$, estimated from ITRS roadmap
7. $C_g=C_{ox}WL=k\varepsilon_0 WL/t_{ox}=3.9\times8.85\times10^{-12}\times100\times10^{-9}\times25\times10^{-9}/1\times10^{-9}=9\times10^{-17}F$. assume W=0.1 μm, ITRS PIDS map gives $7\times10^{-17}F$.
8. junction delay $\tau=C_gV_{dd}/(I_d\times W)= 9\times10^{-17}\times1.1/(1.5\times10^{-3}\times0.1)=0.6$ ps
9. frequency $f=1/\tau=1500$ GHz
10. Power = $I_dV_{dd} = 1.5\times10^{-3}\times0.1/1.1 = 0.15$mW per transistor

Another solution can pick a 90 nm node device performance and then use scaling theory to calculate the device performance.