

- 4.3. As MOS devices are scaled to smaller dimensions, gate oxides must be reduced in thickness.**
- As the gate oxide thickness decreases, do MOS devices become more or less sensitive to sodium contamination? Explain.**
 - As the gate oxide thickness decreases, what must be done to the substrate doping (or alternatively the channel V_{TH} implant, to maintain the same V_{TH} ? Explain.**

Answer:

a). From the text, Na^+ contamination causes threshold voltage instabilities in MOS devices. Also from Eqn. 4.1, the threshold voltage is given by

$$V_{TH} = V_{FB} + 2\phi_f + \frac{\sqrt{2\epsilon_S q N_A (2\phi_f)}}{C_{OX}} + \frac{qQ_M}{C_{OX}}$$

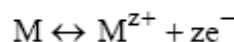
As the gate oxide thickness decreases, C_{OX} increases, so the same amount of mobile charge Q_M will have less effect on V_{TH} as oxides get thinner. Therefore MOS devices are less sensitive to sodium contamination.

b). Using the same expression for V_{TH} as in part a), we observe that as the oxide thickness decreases, (C_{OX} increases), to maintain the same V_{TH} , N_A will have to increase. N_A will actually have to increase by the square root of the oxide thickness decrease to keep V_{TH} constant.

- 4.4. A new cleaning procedure has been proposed which is based on H_2O saturated with O_2 as an oxidant. This has been suggested as a replacement for the H_2O_2 oxidizing solution used in the RCA clean. Suppose a Si wafer, contaminated with trace amounts of Au, Fe and Cu is cleaned in the new H_2O/O_2 solution. Will this clean the wafer effectively? Why or why not? Explain.**

Answer:

As described in the text, cleaning metal ions off of silicon wafers involves the following chemistry:



The cleaning solution must be chosen so that the reaction is driven to the right because this puts the metal ions in solution where they can be rinsed off. Since driving the reaction to the right corresponds to oxidation, we need an oxidizing solution to clean the wafer.

H₂O/O₂ is certainly an oxidizing solution. But whether it cleans effectively or not depends on the standard oxidation potential of the various possible reactions. From Table 4-3 in the text, we have:

Oxidant/ Reductant	Standard Oxidation Potential (volts)	Oxidation-Reduction Reaction
SiO ₂ /Si	0.84	Si + 2H ₂ O ↔ SiO ₂ + 4H ⁺ + 4e ⁻
Fe ³⁺ /Fe	0.17	Fe ↔ Fe ³⁺ + 3e ⁻
Cu ²⁺ /Cu	-0.34	Cu ↔ Cu ²⁺ + 2e ⁻
O ₂ /H ₂ O	-1.23	2H ₂ O ↔ O ₂ + 4H ⁺ + 2e ⁻
Au ³⁺ /Au	-1.42	Au ↔ Au ³⁺ + 3e ⁻

The stronger reactions (dominating) are at the bottom.

Thus the H₂O/O₂ reaction will clean Fe and Cu, but it will not clean Au off the wafer.

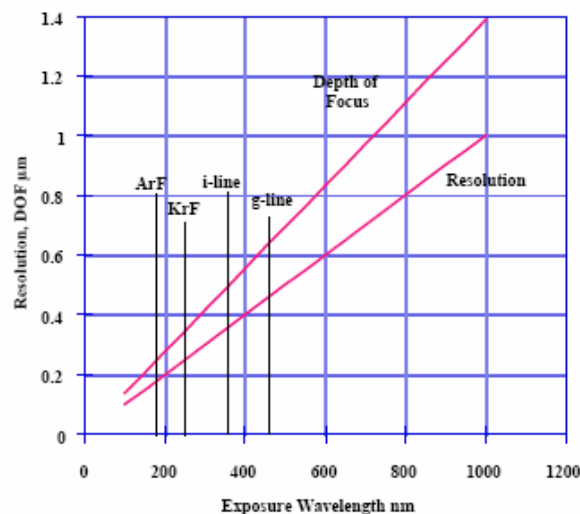
- 5.1. Calculate and plot versus exposure wavelength the theoretical resolution and depth of focus for a projection exposure system with a NA of 0.6 (about the best that can be done today). Assume $k_1 = 0.6$ and $k_2 = 0.5$ (both typical values). Consider wavelengths between 100 nm and 1000 nm (DUV and visible light). Indicate the common exposure wavelengths being used or considered today on your plot (g-line, i-line, KrF and ArF). Will an ArF source be adequate for the 0.13 μm and 0.1 μm technology generations according to these simple calculations?

Answer:

The relevant equations are simply

$$\therefore R = k_1 \frac{\lambda}{\text{NA}} = 0.6 \frac{\lambda}{0.6} \quad \text{and} \quad \text{DOF} = \pm k_2 \frac{\lambda}{(\text{NA})^2} = \pm 0.5 \frac{\lambda}{(0.6)^2}$$

These equations are plotted below. Note that the ArF (193 nm) will not reach 0.13 μm or 0.1 μm resolution according to these simple calculations. In fact, with more sophisticated techniques such as phase shift masks, off axis illumination etc., ArF is expected to reach 0.13 μm and perhaps the 0.1 μm generations.



5.10. Future optical lithography systems will likely use shorter exposure wavelengths to achieve higher resolution and they will also likely use planarization techniques to provide “flat” substrates on which to expose the resist layers. Explain why “flat” substrates will be more important in the future than they have been in the past.

Answer:

As the wavelength of the exposure system decreases, the depth of focus of the exposure system also decreases. Thus it will be necessary to make sure that the resist in which the image is to be exposed, is flat and does not require much depth of focus. Planarization techniques will be required to accomplish this. This could mean CMP to planarize the substrate before the resist is applied, or it could mean using a spun on resist which planarizes the substrate and which is then covered with a thin, uniform imaging resist layer.