Yiorgos Makris – Curriculum Vitae

Contact Information:

- **Address:** Electrical & Computer Engineering Department, University of Texas at Dallas, Richardson, TX 75080, USA
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- **Home Page:** http://www.utdallas.edu/~yiorgos.makris
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- **Personal Data:** Born April 1, 1973, Male, US Citizen, Married to Dr. Una E. Makris, MD.

Research Interests:

- Security and Trustworthiness of Integrated Circuits and Systems
- Applications of Data Analytics in Semiconductor Manufacturing
- Machine Learning-based Test and Calibration of Analog/RF Integrated Circuits
- Hardware-Based Workload Execution Forensics and Malware Detection in Microprocessors
- On-Chip Learning and Intelligent Reconfigurable Computing with Novel Materials and Emerging Technologies
- Workload-Cognizant Resiliency Analysis in Modern Microprocessors
- Test and Reliability of Asynchronous Integrated Circuits
- VLSI Design & Test, Computer-Aided Design, Computer Architecture, Computer Engineering

Education:

- University of California San Diego, CA, USA, Computer Science & Engineering Department, Sep ’95 - Jan ’01
  Ph.D. in Computer Engineering, Jan ’01
  Thesis Title: “Transparency-Based Hierarchical Testability Analysis and Test Generation for RTL Designs”
  Advisor: Dr. Alex Orailoğlu
  C. Phil. in Computer Engineering, Jun ’98
  M.S. in Computer Engineering, Jun ’97

- University of Patras, Greece, Computer Engineering & Informatics Department, Sep ’90 - Jun ’95
  Diploma in Computer Engineering and Informatics, Jun ’95
  Thesis Title: “Built-in Self-Test of Embedded Cache Memories”
  Advisor: Dr. Dimitrios Nikolos

Professional Positions:

- University of Texas at Dallas, Richardson, TX, USA, Sep ’14 - Present, Professor, Electrical & Computer Engineering Department
- University of Texas at Dallas, Richardson, TX, USA, Jul ’11 - Aug ’14, Associate Professor, Electrical & Computer Engineering Department
- Yale University, New Haven, CT, USA, Jan ’06 - Jun ’11, Associate Professor, Electrical Engineering Department
- University of Washington, Seattle, WA, USA, Jan ’05 - Dec ’05, Visiting Faculty, Electrical Engineering Department
- Yale University, New Haven, CT, USA, Jan ’01 - Dec ’05, Assistant Professor, Electrical Engineering Department
- Intel Corp., Portland, OR USA, Jun ’97 - Sep ’97, Sr. CAD Engineer, Design for Test Group
- Intel Corp., Folsom, CA, USA, Jul ’96 - Oct ’96, Summer Intern, Design Technology Group
- University of California San Diego, La Jolla, CA, USA, Sep ’96 - Jun ’00, Research Assistant, Reliable Systems Synthesis Lab
- Bauman Technical University, Moscow, Russia, Jun ’94 - Aug ’94, IAESTE Trainee, Digital Design Lab
- Computer Technology Institute, Patras, Greece, Sep ’93 - Jun ’94, Research Assistant, Digital Design Lab

Sponsored Research (Total: $8.3M):

- **Active ($4.104M):**
  - NSF / IIP, CNS 1747773, “Planning IUCRC: Center for Hardware and Embedded System Security and Trust (CHEST),” 01/01/18 – 12/31/18, (single-PI, $15K)
  - AFRL / Wyle Laboratories FA8075-14-D-0025, “Hardware Trojans in Analog/Mixed-Signal ICs: Risks and Remedies,” 01/03/18 – 08/31/19, (single-PI, $500K)

- Texas Instruments, "Towards DPPB-level Quality in Analog ICs: Detecting Intricate Defects through On-Die Design-Specific Process Control Monitors," 04/01/18 – 03/31/21, (single-PI, $240K) (in contract negotiation)
- Advantest Corp., Gift to support research in "Applications of Machine Learning in Test," 03/01/18 – 2/28/10 (single-PI, $40K)
- ams AG, "Machine Learning-Based Solutions for Automated Die-Inking," 03/01/18 – 2/28/19, (single-PI, $85K) (in contract negotiation)
- DARPA HR001116S0001-FP39, "ECLIPSE: Efficient Cross-Layered IP Protection SchemE," 03/01/18 – 08/31/19, (PI: Farinaz Koushanfar, co-PIs: Jeyavijayan Rajendran, Ozgur Sinanoglu, Yiorgos Makris, $635K)
- Texas Instruments Foundational Technology Research Center (FTRC) on Millimeter-Wave and High Frequency Microsystems (HFM), "Advanced Algorithms for THz Sensing and Recognition," 10/01/17 – 09/30/21 (PI: Murat Torlak, co-PI: Yiorgos Makris, $500K)
- Texas Instruments / UTD TxACE, "Adaptive Testing and Trimming of Analog/RF ICs," 08/01/17 – 07/31/20 (single-PI, $230K, including overhead waiver contribution of $80K by University of Texas at Dallas)
- SRC 2709.001, "Post-Silicon Layout Sensitivity Mining: A Pathway to Defect-Driven Test Quality," 11/1/16-10/31/19 (single-PI, $267K)
- NSF 1735673, "Student Travel Support for 2017 IEEE VLSI Test Symposium," 07/01/17 – 06/30/18 (single-PI: $12K)
- NSF / CISE, CNS 1514050, "TWC: Medium: Hardware Trojans in Wireless Networks - Risks and Remedies," 09/01/15 – 08/31/19 (PI: Yiorgos Makris, co-PI: Aria Nosratinia, $1.13M)
- NSF / CISE, CCF 1527460 & SRC 2625.001, "SHF: Small: On-Die Learning: A Pathway to Post-Deployment Robustness and Trustworthiness of Analog/RF ICs," 09/01/15 – 08/31/18 (single-PI, $450K ($350K + $100K))

- **Completed ($4.196M):**
  - NSF 1675371, "Student Travel Support for 2016 IEEE VLSI Test Symposium," 07/01/16 – 06/30/17 (single-PI: $12K)
  - SRC/TxACE 1836.131, "Process Variation Anatomy: A Statistical Nexus between Design, Manufacturing and Test," 10/01/13 – 09/30/16 (single-PI, $330K)
  - NSF / CISE, CNS 1311860 & 1319105, "TWC: Small: Collaborative: Toward Trusted 3rd-Party Microprocessor Cores: A Proof Carrying Code Approach," 10/01/13 – 09/30/16 (PI: Yier Jin, co-PI: Yiorgos Makris, $460K ($243K + $217K))
  - NSF / CISE, CCF 1255754 & SRC 2413.001, Joint Effort on Failure Resistant Systems, "Cross-Layer Intelligent System-Based Adaptive Power Conditioning for Robust and Reliable Mixed-Signal Multi-Core SoCs," 04/01/13 – 03/31/16 (PI: Yiorgos Makris, co-PI: Dongsheng Ma, $320K ($192K + $128K))
  - ARO / CS, 60709, "Trusted Module Acquisition Through Proof-Carrying Hardware Intellectual Property," 02/01/12 – 01/31/15 (single-PI, $330K)
  - Intel Corp., Gift to support research in "Information-Rich Sample Selection Based on Wafer-Level Spatial Variation Analysis," 11/01/13 – 10/31/14 (single-PI, $30K)
  - NSF / CISE, CNS 1017719 (transferred to UT Dallas as NSF /CISE, CNS 1149465), "TC: Small: THWART: Trojan Hardware in Wireless ICs - Analysis and Remedies for Trust," 09/01/10 – 08/31/14 (single-PI, $500K)
  - NSF / CISE, CNS 1439720, "REU Supplement to TC: Small: THWART: Trojan Hardware in Wireless ICs - Analysis and Remedies for Trust," 06/01/14 – 08/31/14 (single-PI, $8K)
  - The University of Texas at Dallas, Lab Setup Fund, 07/01/11 – 08/31/14, $175K
  - SRC/TxACE, TJ 1836.092 "A Model View Controller (MVC) Framework for Adaptive Test," 08/01/10 – 07/31/13 (single-PI, $300K)
  - NSF / CISE, CCF 0916803 & CCF 0916415 (transferred to UT Dallas as NSF /CISE, CCF 1149463), "SHF: Small: Collaborative Research: Correlation Mining and its Applications in Test Cost Reduction, Yield Enhancement, and Performance Calibration in Analog/RF Circuits," 09/01/09 – 08/31/12 (PI: Yiorgos Makris, co-PI: Petros Drineas, $450K ($240K + $210K))
  - Graduate Student Fellowship to Mr. Nathan Kupp, linked to SRC, TJ 2012 "A Model View Controller (MVC) Framework for Adaptive Test," 09/01/08 – 08/31/12 (single-PI, $210K)
  - NSF / CISE, CNS 1132205, "REU Supplement to TC: Small: THWART: Trojan Hardware in Wireless ICs - Analysis and Remedies for Trust," 06/01/11 – 08/31/11 (single-PI, $8K)
  - NSF / CISE, CCF 1132204, "REU Supplement to Correlation Mining and its Applications in Test Cost Reduction, Yield Enhancement, and Performance Calibration in Analog/RF Circuits," 06/01/11 – 08/31/11 (single-PI, $8K)
  - NSF / CISE, CCF 1039388, "REU Supplement to Correlation Mining and its Applications in Test Cost Reduction, Yield Enhancement, and Performance Calibration in Analog/RF Circuits," 06/01/10 – 08/31/10 (single-PI, $8K)
  - SRC/TxACE, TJ 1836.029, "Statistical Analysis of Parametric Measurements and its Applications in Analog/RF Test," 08/01/09 – 07/31/10 (single-PI, $82K, including overhead waiver contribution of $32K by Yale University)

- NSF / ENG, ECCS 0936674, "REU Supplement to GOALI: A Machine-Learning Approach to Built-In Self-Test of Analog/RF Circuits," 06/01/09 – 08/31/09 (single-PI, $6K)
- Intel Corp., Equipment Donation to support research in "Concurrent Error Detection in Microprocessor Controllers," 07/01/08 (single-PI, $12K)
- NSF / CISE, CCF 0702522, "Concurrent Error Detection in Analog Circuits," 07/01/07 – 06/30/10 (single-PI, $120K)
- NSF / CISE, CCF 0834846, "REU Supplement to Concurrent Error Detection in Analog Circuits," 06/01/08 – 08/31/08 (single-PI, $6K)
- NSF / ENG, ECCS 0622081, "GOALI: A Machine-Learning Approach to Built-In Self-Test of Analog/RF Circuits," 09/01/06 – 08/31/09 (single-PI, $270K)
- NSF / ENG, ECCS 0735019, "REU Supplement to GOALI: A Machine-Learning Approach to Built-In Self-Test of Analog/RF Circuits," 07/01/07 – 08/31/07 (single-PI, $6K)
- SRC, TJ 1632.001, "Statistical Analysis of Parametric Measurements and its Applications in Analog/RF Test," 08/01/07 – 07/31/09 (single-PI, $165K, including overhead waiver contribution of $65K by Yale University)
- Intel Corp., Gift to support research in "Concurrent Error Detection in Microprocessor Controllers," 07/01/07 – 06/31/10 (single-PI, $150K)
- DARPA / Boeing, KT 3425, "A Testability Study for the Asynchronous Circuits of the CLASS Program," 01/01/06 – 12/31/06 (single-PI, $30K)
- Stavros S. Niarchos Faculty Research Grant, "Who-is-who in Hi-Tech in Greece", 06/01/03 – 08/31/03 (single-PI, $8K)
- Yale University, Lab Setup & Research Initiation Fund, 01/01/01 – 12/31/05 ($192K)

Awards and Honors:

- Best Paper in Session Award (Advisee: Gaurav Rajavendra Reddy), TECHCON, Sep '17
- Best Hardware Demonstration Award, IEEE International Hardware Oriented Security and Trust Symposium (HOST) (Advisee: Yu Liu), May '16
- Winners of Embedded Systems Challenge (ESC) at NYU Cyber-Security Awareness Week (CSAW) (Advisees: Mahdi Bidmeshki, Gaurav Rajavendra and Liwei Zhou), Nov '15
- Best Paper Award, IEEE VLSI Test Symposium (VTS), Apr '15
- Best Paper Award, IEEE Design Automation and Test in Europe Conference (DATE), Mar '13
- 2012 E.J. McCluskey Best Doctoral Thesis Award, IEEE Test Technology Council (Advisee: Nathan Kupp), Nov '12
- Winners of Embedded Systems Challenge (ESC) at NYU Cyber-Security Awareness Week (CSAW) (Advisees: Yier Jin and Michail Maniatakos), Oct '11
- Best Paper in Session Award (Advisee: Nathan Kupp), TECHCON, Sep '11
- Best Student Paper Award (Advisee: Nathan Kupp), IMS3TW, May '11
- IEEE Computer Society, Golden Core Member, Apr '10
- IEEE Computer Society, Meritorious Service Award, Apr '10
- National Academy of Engineering (NAE) Frontiers of Engineering Symposium Participant, Sep '07
- IEEE Computer Society, Certificate of Appreciation, Oct '06, Oct '08
- Sheffield Distinguished Teaching Award, Faculty of Engineering, Yale University, May '06
- Yale University, Junior Faculty Fellowship, Jan '05 - Dec '05
- Paul Moore Award for Developing Course *"Semiconductors, Computers and Communications"*, May '03 ($10K)
- Paul Moore Award for Developing Course *"Digital Systems Testing And Design for Testability"*, May '01 ($11K)
- INTEL Corp. Recognition Award, Sep '96
- UCSD School of Engineering Industrial Fellowship, Sep '95 - Dec '95
- University of Patras, Honors Graduate, Jun '95

Book Chapters:

[1] A. Elfadel, D. Bonning and X. Li (Editors), "Machine Learning in VLSI Computer-Aided Design," *Springer*, 2018 (N. Kupp, K. Huang, A. Ahmadi, C. Xanthopoulos and **Y. Makris**, "Gaussian Process-Based Wafer-Level Correlation Modeling and its Applications") (invited – to appear)

[2] S. Bhunia and M. Tehranipoor (Editors), "The Hardware Trojan War: Attacks, Myths, and Defenses," *Springer*, 2017 (A. Antonopoulos, C. Kapatsori, **Y. Makris**, "Hardware Trojans in Analog, Mixed-Signal and RF ICs") (invited)

[3] C. H. Chang, M. Potkonjak (Editors), "Secure System Design and Trustable Computing" *Springer*, 2015 (Y. Jin, D. Maliuk, **Y. Makris**, "Hardware Trojan Detection in Analog/RF Integrated Circuits") (invited)

[4] T. Noulis, M. Soma (Editors), "Mixed-Signal Circuits," *CRC Press*, 2015 (D. Maliuk, H. Stratigopoulos, **Y. Makris**, "Machine Learning-Based BIST in Analog/RF ICs") (invited)

[5] M. Tehranipoor, C. Wang (Editors), "Introduction to Hardware Security and Trust," *Springer*, 2011 (Y. Jin, E. Love, **Y. Makris**, "Design for Hardware Trust") (invited)

[6] K. Iniewski (Editor), "Advanced Circuits for Emerging Technologies," *John Wiley & Sons*, 2012 (H. Stratigopoulos, **Y. Makris**, "Checkers for On-line Self-Testing of Analog Circuits") (invited)

[7] L. T. Wang, C. E. Stroud, and N. A. Touba (Editors), "System on-Chip Test Architectures," *Morgan-Kaufman Publishers*, 2007 (**Y. Makris**, section 8.4, "Circuit-Level Approaches to Soft Error Mitigation") (invited)

Journal Publications:

[8] A. Antonopoulos, C. Kapatsori, **Y. Makris,** "Trusted Analog/Mixed-Signal/RF ICs: A Survey and a Perspective," *IEEE Design & Test of Computers (D&T)*, vol. 34, no. 6, pp. 63-76, 2017

[9] A. Ahmadi, H.-G. Stratigopoulos, K. Huang, A. Nahar, B. Orr, M. Pas, J. M. Carulli, **Y. Makris**, "Yield Forecasting Across Semiconductor Fabrication Plants and Design Generations," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (T. CAD)*, vol. 36, no. 12, pp. 2120-2133, 2017

[10] Y. Jin, X. Guo, R. G. Dutta, M. Bidmeshki, **Y. Makris**, "Data Secrecy Protection through Information Flow Tracking in Proof-Carrying Hardware IP (Part I: Framework Fundamentals)," *IEEE Transactions on Information Forensics and Security (T.IFS)*, vol. 12, no. 10, pp. 2416-2429, 2017

[11] M. Bidmeshki, X. Guo, R. G. Dutta, Y. Jin, **Y. Makris**, "Data Secrecy Protection through Information Flow Tracking in Proof-Carrying Hardware IP (Part II: Framework Automation)," *IEEE Transactions on Information Forensics and Security (T.IFS)*, vol. 12, no. 10, pp. 2430-2443, 2017.

[12] Y. Liu, Y. Jin, A. Nosratinia, **Y. Makris**, "Silicon Demonstration of Hardware Trojan Design and Detection in Wireless Cryptographic ICs," *IEEE Transactions on Very Large Scale Integration (T.VLSI)*, vol. 25, no. 4, pp. 1506-1519, 2017

[13] G. Volanis, A. Antonopoulos, A. Hatzopoulos, **Y. Makris**, "Toward Silicon-Based Cognitive Neuromorphic ICs - A Survey," *IEEE Design & Test of Computers (D&T)*, vol. 33, no. 3, pp. 91-102, 2016

[14] M. Maniatakos, M. Michael, **Y. Makris**, "Multiple-Bit Upset Protection in Microprocessor Memory Arrays using Vulnerability-based Parity Optimization and Interleaving," *IEEE Transactions on Very Large Scale of Integration Systems (T.VLSI)*, vol. 23, no. 11, pp. 2447-2460, 2015

[15] M. Maniatakos, M. Michael, C. Tirumurti, **Y. Makris**, "Revisiting Vulnerability Analysis in Modern Microprocessors," *IEEE Transactions on Computers (TCOMP)*, vol. 64, no. 9, pp. 2664-2674, 2015

[16] D. Maliuk, **Y. Makris**, "An Experimentation Platform for On-chip Integration of Analog Neural Networks: A Pathway to Trusted and Robust Analog/RF ICs," *IEEE Transactions on Neural Networks and Learning Systems (T.NNLS)*, vol. 26, no. 8, pp. 1721-1734, 2015

[17] K. Huang, N. Korolja, J. M. Carulli Jr., **Y. Makris,** "Recycled IC Detection based on Statistical Methods," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (T. CAD)*, vol. 34, no. 6, pp. 947-960, 2015

[18] K. Huang, N. Kupp, C. Xanthopoulos, J. M. Carulli Jr., **Y. Makris**, "Low-Cost Analog/RF IC Testing through Combined Intra- and Inter-Die Correlation Models," *Special Issue on Speeding up Analog Integration and Test for Mixed-signal SOCs of the IEEE Design & Test of Computers (D&T)*, vol. 32, no. 1, pp. 53-60, 2015

[19] U. Guinn, K. Huang, D. DiMase, J. M. Carulli Jr., M. Tehranipoor, **Y. Makris**, "Counterfeit Integrated Circuits: A Rising Threat in the Global Semiconductor Supply Chain," *Proceedings of the IEEE (P.IEEE)*, vol. 102, no. 8, pp. 1207-1228, 2014

[20] N. Karimi, M. Maniatakos, C. Tirumurti, **Y. Makris**, "On the Impact of Performance Faults in Modern Microprocessors," *Journal of Electronic Testing: Theory & Applications (JETTA)*, Springer, vol. 29, no. 3, pp. 351-366, 2013

[21] M. Maniatakos, P. Kudva, B. Fleischer, **Y. Makris,** "Low-cost Concurrent Error Detection for Floating Point Unit (FPU) Controllers," *IEEE Transactions on Computers (T.COMP)*, vol. 62, no. 7, pp. 1376-1388, 2013

[22] M. Maniatakos, C. Tirumurti, **Y. Makris**, "Global Signal Vulnerability (GSV) Analysis for Selective State Element Hardening on Modern Microprocessors," *IEEE Transactions on Computers (T.COMP)*, vol. 61, no. 9, pp. 1361-1370, 2012

[23] N. Kupp, **Y. Makris**, "Applying the Model-View-Controller Paradigm to Adaptive Test," *Special Issue on Yield Learning of the IEEE Design and Test of Computers (D&T)*, vol. 29, no. 1, pp. 28-35, 2012

[24] E. Love, Y. Jin, **Y. Makris**, "Proof-Carrying Hardware Intellectual Property: A Pathway to Trusted Module Acquisition," *Special Issue on Integrated Circuits and System Security of the IEEE Transactions on Information Forensics and Security (T.IFS)*, vol. 7, no. 1, pp. 25-40, 2012

[25] N. Karimi, M. Maniatakos, C. Tirumurti, A. Jas, **Y. Makris**, "A Workload-Cognizant Concurrent Error Detection Method for a Modern Microprocessor Controller," *Special issue of IEEE Transactions on Computers (T.COMP) on Concurrent On-Line Testing and Error/Fault Resilience of Digital Systems*, vol. 60, no. 9, pp. 1174-1187, 2011

[26] M. Maniatakos, N. Karimi, C. Tirumurti, A. Jas, **Y. Makris**, "Instruction-Level Impact Analysis of Low-Level Errors in a Modern Microprocessor Controller," *Special issue of IEEE Transactions on Computers (T.COMP) on Concurrent On-Line Testing and Error/Fault Resilience of Digital Systems*, vol. 60, no. 9, pp. 1160-1173, 2011

[27] N. Kupp, H. Huang, P. Drineas, **Y. Makris**, "Cost-Benefit Analysis of Post-Production Performance Calibration in Analog/RF Devices," *IEEE Design and Test of Computers (D&T),* vol. 28, no.3, pp. 64-75, 2011

[28] Y. Jin, **Y. Makris**, "Hardware Trojans in Wireless Cryptographic Integrated Circuits," *Special issue of IEEE Design & Test of Computers (D&T) on Verifying Physical Trustworthiness of Integrated Circuits and Systems,* vol. 27, no. 1, pp. 26-35, 2010

[29] H-G. Stratigopoulos, P. Drineas, M. Slamani, **Y. Makris**, "RF Specification Test Compaction using Learning Machines," *IEEE Transactions on Very Large Scale Integration (T.VLSI)*, vol. 18, no. 6, pp. 1002-1006, 2010

[30] N. Kupp, P. Drineas, M. Slamani, **Y. Makris**, "On Boosting the Accuracy of Non-RF to RF Correlation-Based Specification Test Compaction," *Journal of Electronic Testing Theory and Applications (JETTA), Springer,* vol. 25, no. 6, pp. 309-321, 2009

[31] S. Almukhaizim, P. Drineas, **Y. Makris**, "Parity-Based Concurrent Error Detection with Bounded-Latency in Finite State Machines," *Kuwait Journal of Science and Engineering (KJSE)*, vol. 36, no. 2B, pp. 141-162, 2009

[32] S. Almukhaizim, F. Shi, E. Love, **Y. Makris**, "Soft Error Tolerance and Mitigation in Asynchronous Burst Mode Circuits," *IEEE Transactions on Very Large Scale Integration (T.VLSI)*, vol. 17, no. 7, pp. 869-882, 2009

[33] F. Shi, **Y. Makris**, "Enhancing Simulation Accuracy through Advanced Hazard Detection in Asynchronous Circuits," *IEEE Transactions on Computers (T.COMP),* vol. 58, no. 3, pp. 394-408, 2009

[34] H-G. D. Stratigopoulos, **Y. Makris**, "Error Moderation in Low-Cost Machine Learning-Based Analog/RF Testing," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (T. CAD)*, vol. 27, no. 2, pp. 339-351, 2008

[35] S. Almukhaizim, **Y. Makris**, "A Novel Soft Error Rate (SER) Reduction Methodology through Addition of Gate-Level Functional Redundancy," *IEEE Transactions on Reliability (T. REL),* vol. 57, no. 1, pp. 23-31, 2008

[36] S. Almukhaizim, **Y. Makris**, "Concurrent Error Detection Methods for Asynchronous Burst Mode Machines," *IEEE Transactions on Computers (T. COMP),* vol. 56, no. 6, pp. 785-798, 2007

[37] **Y. Makris**, A. Orailoğlu, "On the Identification of Modular Test Requirements for Low-Cost Hierarchical Test Path Construction," *Integration: The VLSI Journal (JVLSI)*, Elsevier, vol. 40, no. 3, pp. 315-325, 2007

[38] H-G. D. Stratigopoulos, **Y. Makris**, "An Adaptive Checker for the Fully Differential Analog Code," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 41, no. 6, pp. 1421-1429, 2006

[39] S. Almukhaizim, P. Drineas, **Y. Makris**, "Entropy-Driven Parity Tree Selection for Low-Cost Concurrent Error Detection," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (T. CAD)*, vol. 25, no. 8, pp. 1547-1554, 2006

[40] H-G. D. Stratigopoulos, **Y. Makris**, "Concurrent Error Detection in Linear Analog Circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (T. CAD)*, vol. 25, no. 5, pp. 878-891, 2006

[41] H-G. D. Stratigopoulos, **Y. Makris**, "Non-Linear Decision Boundaries for Testing Analog Circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (T. CAD)*, vol. 24, no. 11, pp. 1760-1773, 2005

[42] S. Almukhaizim, P. Drineas, **Y. Makris**, "Compaction-Based Concurrent Error Detection for Digital Circuits," *Microelectronics Journal (MJ)*, Elsevier, vol. 36, no. 9, pp. 856-862, 2005

[43] H-G. D. Stratigopoulos, **Y. Makris**, "An Analog Checker with Input-Relative Tolerance for Duplicate Signals," *Journal of Electronic Testing: Theory & Applications (JETTA),* Kluwer Academic Publishers (now Springer), vol. 20, no. 5, pp. 479-488, 2004

[44] **Y. Makris**, I. Bayraktaroğlu, A. Orailoğlu, "Enhancing Reliability of RTL Controller-Datapath Circuits via Invariant-Based Concurrent Test," *IEEE Transactions on Reliability (T. REL)*, vol. 53, no. 2, pp. 269-278, 2004

[45] P. Drineas, **Y. Makris**, "SPaRe: Selective Partial Replication for Concurrent Fault Detection in FSMs," *IEEE Transactions on Instrumentation and Measurement (T. I &M),* vol. 52, no. 6, pp. 1729-1737, 2003

[46] **Y. Makris**, J. Collins, A. Orailoğlu, "Fast Hierarchical Test Path Construction for Circuits with DFT-Free Controller-Datapath Interface," *Journal of Electronic Testing: Theory & Applications (JETTA),* Kluwer Academic Publishers (now Springer), vol. 18, no. 1, pp. 29-42, 2001

[47] **Y. Makris**, A. Orailoğlu, "RTL Test Justification and Propagation Analysis for Modular Designs*," Journal of Electronic Testing: Theory & Applications (JETTA),* Kluwer Academic Publishers (now Springer), vol. 13, no. 2, pp. 105-120, 1998

Conference Publications:

[48] G. Rajavendra Reddy, C. Xanthopoulos, **Y. Makris**, "Enhanced Hotspot Detection Through Synthetic Pattern Generation and Design of Experiments," *Proceedings of the IEEE VLSI Test Symposium (VTS)*, 2018 (to appear)

[49] L. Zhou, **Y. Makris**, "Hardware-Assisted Rootkit Detection via On-line Statistical Fingerprinting of Process Execution," *Proceedings of the IEEE Design Automation and Test in Europe Conference (DATE)*, 2018 (to appear)

[50] M. Zaman, A. Sengupta, D. Liu, O. Sinanoglu, **Y. Makris,** J. Rajendran, "Towards Provably-Secure Performance Locking," *Proceedings of the IEEE Design Automation and Test in Europe Conference (DATE)*, 2018 (to appear)

[51] K. Subramani, A. Antonopoulos, A. Abotabl, A. Nosratinia, **Y. Makris**, "ACE: Adaptive Channel Estimation for Detecting Analog/RF Trojans in WLAN Transceivers," *Proceedings of the IEEE International Conference on Computer-Aided Design (ICCAD)*, pp. 722-727, 2017

[52] C. Xanthopoulos, P. Sarson, H Reiter, **Y. Makris**, "Automated Die Inking: A Pattern Recognition-Based Approach," *Proceedings of the IEEE International Test Conference (ITC)*, pp. 12.1.1-12.1.6, 2017

[53] G. Rajavendra Reddy, C. Xanthopoulos, **Y. Makris**, "Enhanced Hotspot Detection Through Synthetic Hotspot Generation and Design of Experiments," *Proceedings of the SRC Technology and Talent for the 21st Century Conference (TECHCON)*, pp. 1-4, 2017 **(Best-in-Session Award)**

[54] C. Xanthopoulos, A. Ahmadi, S. Boddikurapati, A. Nahar, B. Orr, **Y. Makris**, "Wafer-Level Adaptive Trim Seed Forecasting," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, 2017

[55] A. Antonopoulos, C. Kapatsori, **Y. Makris,** "Security and Trust in the Analog/Mixed-Signal/RF Domain: A Survey and a Perspective," *Proceedings of the IEEE European Test Symposium (ETS)*, pp. 1-10, 2017

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[174] **Y. Makris**, J. Collins, A. Orailoğlu, P. Vishakantaiah, "TRANSPARENT: A System for RTL Testability Analysis, DFT Guidance and Hierarchical Test Generation," *Proceedings of the IEEE Custom Integrated Circuits Conference (CICC)*, pp. 159-162, 1999

[175] **Y. Makris**, A. Orailoğlu, "Channel-Based Behavioral Test Synthesis for Improved Module Reachability," *Proceedings of the IEEE Design Automation and Test in Europe Conference (DATE)*, pp. 283-288, 1999

[176] **Y. Makris**, A. Orailoğlu, "DFT Guidance Through RTL Test Justification and Propagation Analysis," *Proceedings of the IEEE International Test Conference (ITC)*, pp. 668-677, 1998

Workshop Papers:

[177] D. Maliuk, Y. Makris, "Analog Implementation of Ontogenic Neural Networks for RF Built-In Self-Test," *Presented at the IEEE Test and Validation of High-Speed Analog Circuits,* Anaheim, CA, USA, Sep '13

[178] S. Almukhaizim, P. Drineas, **Y. Makris**, "Roving Concurrent Error Detection for Logic Circuits," *Presented at the IEEE North Atlantic Test Workshop,* Essex Junction, VT, USA, May '04

[179] S. Almukhaizim, **Y. Makris**, "Fault Tolerant Design of Random Logic based on a Parity Check Code," *Presented at the IEEE European Test Workshop*, Maastricht, Netherlands, May '03

[180] P. Drineas, **Y. Makris**, "On the Compaction of Independent Test Sequences for Sequential Circuits," *Presented at the IEEE European Test Workshop*, Maastricht, Netherlands, May '03

[181] **Y. Makris**, A. Orailoğlu, "Reducing Hierarchical Test Path Cost via Modular Test Requirement Analysis," *Presented at the IEEE European Test Workshop,* Corfu, Greece, May '02

[182] P. Drineas, **Y. Makris**, "Non-Intrusive Design of Concurrently Self-Testable FSMs," *Presented at the IEEE North Atlantic Test Workshop,* Montauk, NY, USA, May '02

[183] **Y. Makris**, A. Orailoğlu, "Test Requirement Analysis for Low Cost Hierarchical Test Path Construction," *Presented at the IEEE International Workshop of RTL Test Generation,* Nara, Japan, Nov '01

[184] **Y. Makris**, J. Collins, A. Orailoğlu, "How to Avoid Random Walks in Hierarchical Test Path Identification," *Presented at the IEEE European Test Workshop,* Cascais, Portugal, May '00

[185] **Y. Makris**, A. Orailoğlu, "Exploiting Off-Line Hierarchical Test Paths in Module Diagnosis and On-Line Test," *Presented at the IEEE Latin American Test Workshop,* Rio de Janeiro, Brazil, Feb '00

[186] **Y. Makris**, A. Orailoğlu, "Property-Based RTL Test Justification and Propagation Analysis," *Presented at the IEEE International Test Synthesis Workshop*, Santa Barbara, CA, USA, Mar '98

Invited Presentations:

- "An Overview of Hardware Security Research at UT Dallas' Trusted and RELiable Architectures (TRELA) Laboratory,"
  - *Invited Seminar at Air Force Research Laboratory (AFRL),* Dayton, OH, Dec '17 (Host: L. Orlando)
- "Applications of Machine Learning in Hardware Security,"
  - *Departmental Seminar, University of California, Berkeley*, Berkeley, CA, Dec '17 (Host: J. Roychowdhury)
- "Enhanced Lithographic Hotspot Detection Through Design of Experiments,"
  - *Special Session on Machine Learning in Testing Applications, IEEE International Test Conference,* Fort Worth, TX, Oct '17 (Host: P. Song)
- "Machine Learning Applications in Semiconductor Design, Test & Yield Learning,"
  - *GlobalFoundries,* Malta, NY, Aug '17 (Host: R. Desineni)
- "Between a Rock and a Hard Place: Realities of Developing Formal Hardware Security and Trust Solutions,"
  - *Keynote Address, IEEE International Verification and Security Workshop (IVSW),* Thessaloniki, Greece, Jul '17 (Host: M. Abadir)
- "Toward Silicon-Based Cognitive Neuromorphic ICs,"
  - *Invited Tutorial, IEEE International Mixed-Signal Test Workshop (IMSTW),* Thessaloniki, Greece, Jul '17 (Host: M. Barragan)
  - *Embedded Tutorial, IEEE European Test Symposium (ETS),* Limassol, Cyprus, May '17 (Host: G. DiNatale)
- "Security and Trust in the Analog/Mixed-Signal/RF Domain: A Survey and a Perspective,"
  - *Tutorial, IEEE International Symposium on Hardware Oriented Security and Trust (HOST),* McLean, VA, May '17 (Host: D. Forte)
- "Proof-Carrying Hardware Intellectual Property (PCHIP),"
  - *DARPA IP Theft Workshop,* Arlington, VA, Feb '16 (Host: K. Bernstein)
- "Applications of Machine Learning in the Design of Trusted and Reliable Analog/RF ICs,"
  - *Test Spring School,* Nicosia, Cyprus, May '17 (Host: H.-J. Wunderlich)
  - *Departmental Colloquium, University of Washington*, Seattle, WA, Dec '15 (Host: M. Soma)
  - *Aristotle University of Thessaloniki,* Thessaloniki, Greece, Mar '15 (Host: A. Hatzopoulos)
- "Hardware-Induced Security and Privacy Vulnerabilities in IoT,"
  - *Invited Talk at AT&T Foundry,* Richardson, TX, Nov '15 (Host: C. Lee)
- "Hardware Trojans in Wireless Cryptographic ICs,"
  - *Invited Talk at Foundations of Analog Circuits (FAC) Workshop,* Austin, TX, Nov '15 (Host: X. Li)
  - *Invited Talk at IEEE Computer Society Chapter,* Raleigh, NC, Oct '15 (Host: C. Wang)
- "From Data to Actions: Applications of Data Analytics in Semiconductor Manufacturing and Test,"
  - *Tutorial, IEEE International Test Conference (ITC),* Fort Worth, TX, Nov '17 (Host: P. Bernardi)
  - *Tutorial, IEEE Design Automation and Test in Europe (DATE) Conference,* Lausanne, Switzerland, Mar '17 (Host: F. Fummi)
  - *Tutorial, IEEE International Test Conference (ITC),* Fort Worth, TX, Nov '16 (Host: P. Bernardi)

- *Tutorial, IEEE International Test Conference (ITC),* Anaheim, CA, Oct '15 (Host: P. Bernardi)
- *Tutorial, IEEE International Symposium on Circuits and Systems (ISCAS),* Lisbon, Portugal, May '15 (Host: J. De La Rosa)
- *Tutorial, IEEE Design Automation and Test in Europe (DATE) Conference,* Grenoble, France, Mar '15 (Host: F. Fummi)

- "Towards Automatic Proof Generation for Information Flow Policies in Third-Party Hardware Intellectual Property,"
  - *ARO Workshop on Trustworthy Hardware*, New York, NY, Nov '14 (Host: M. Maniatakos)
- "Hardware Security: Building Trustworthy Systems,"
  - *Pavilion Panel at Design Automation Conference*, San Francisco, CA, Jun '14 (Host: B. Cline)
- "Hardware Trojans in Wireless Cryptographic ICs: How Can Test Help?,"
  - *Invited Talk at Southwest Design for Test Conference*, Austin, TX, May '14 (Host: J. Johnson)
- "Laser Trimming Speedup Through Gaussian Process Modeling,"
  - *Texas Instruments,* Freising, Germany, Mar '14 (Host: H. Blank)
- "From Data to Actions: Challenges in Developing & Deploying Statistical Methods in IC Manufacturing & Test,"
  - *Keynote Address, Texas Instruments Data Analytics Workshop,* Plano, TX, Mar '14 (Host: J. Roehr)
- "Too High Frequency to Test - What is the Quality Impact?"
  - *Panelist, 3rd IEEE Test and Validation of High-Speed Analog Circuits Workshop (TVHSAC),* Anaheim, CA, Sep '13 (Host: S. Sunter)
- "Parametric Counterfeit IC Detection via Support Vector Machines,"
  - *NYU-Abu Dhabi "Do you Trust Your Chip?" Workshop,* New York, NY, Apr '13 (Host: M. Maniatakos)
- "Spatial Wafer-Level Correlation Modeling for Test Cost Reduction in Analog/RF Circuits,"
  - *Freescale Semiconductor*, Austin, TX, April '13 (Host: R. Raina)
  - *Intel Corp*, Santa Clara, CA, March '13 (Host: S. Natarajan)
  - *Invited Talk, 2nd IEEE International Workshop on Defect and Adaptive Test Analysis (DATA),* Anaheim, CA, Nov '12 (Host: A. Sinha)
  - *TxACE Weekly Meeting, University of Texas at Dallas,* Richardson, TX, Nov '12 (Host: K. O)
- "Hardware Security and Trust,"
  - *Tutorial, IEEE International Test Conference (ITC),* Seattle, WA, Sep '14 (Host: P. Bernardi)
  - *Tutorial, IEEE Design Automation and Test in Europe (DATE) Conference,* Grenoble, France, Mar '13 (Host: F. Fummi)
  - Texas Security Awareness Week (TexSAW), Richardson, TX, Oct '12 (Host: J. Shapiro)
  - *Tutorial, IEEE International Conference on Computer Design (ICCD),* Montreal, Canada, Sep '12 (Host: S. Tahar)
- "A Model-View-Controller (MVC) Framework for Adaptive Test,"
  - *TxACE E-Seminar, University of Texas at Dallas,* Richardson, TX, Nov '11 (Host: K. O)
- "On-Chip Neural Classifiers for Post-Deployment Trust Monitoring in Wireless Cryptographic ICs,"
  - *Elevator Talks at the International Test Conference*, Anaheim, CA, Sep '11 (Host: S. Mitra)
- "Post-Production Performance Calibration in Analog/RF ICs,"
  - *TxACE Weekly Meeting, University of Texas at Dallas,* Richardson, TX, Sep '11 (Host: K. O)
- "Post-Deployment Trust Monitoring in Wireless Cryptographic ICs,"
  - *NYU-Abu Dhabi "Do you Trust Your Chip?" Workshop,* New York, NY, Apr '11 (Host: O. Sinanoglu)
- "Proof-Carrying Hardware Intellectual Property: A Pathway to Trusted Module Acquisition,"
  - *ARO Workshop on Trusted Hardware,* Arlington, VA, Apr '11 (Hosts: C. Wang & M. Tehranipoor)
- "Trusted Integrated Circuits: Challenges & Opportunities Ahead,"
  - *University of Belgrade,* Belgrade, Serbia, Mar '13 (Host: I. Tartalja)
  - *Technical University of Crete*, Chania, Greece, Mar '13 (Host: A. Dollas)
  - *National Technical University of Athens*, Athens, Greece, Mar '13 (Host: Y. Papananos)
  - *University of Athens*, Athens, Greece, Mar '13 (Host: D. Gizopoulos)
  - *University of Texas*, Dallas, TX, Mar '11 (Host: N. Al-Dhahir)
- "A Machine Learning Approach to Robust Analog/RF Integrated Circuits,"
  - *Brown University*, Providence, RI, Mar '11 (Host: I. Bahar)
  - *University of New Mexico*, Albuquerque, NM, Mar '11 (Host: P. Zarkesh-Ha)
- "Low-Cost Testing for mmWave Test Devices: A Case Study,"
  - *Invited Address at the 2nd International Workshop on Testing and Validation of High-Speed Analog Circuits (TVHSAC'10)*, Austin, TX, Nov'10 (Host: S. Tabatabaei)
- "Hardware Trojans in Wireless Cryptographic Integrated Circuits,"
  - *Microsoft Research*, Bellevue, WA, Sep '10 (Host: D. Lymberopoulos)
  - *Applied Physics Laboratory at Johns Hopkins University (JHU/APL),* Laurel, MD, Jan '10 (Host: D. Wilt)
  - *Elevator Talks at the International Test Conference*, Austin, TX, Nov '09 (Host: S. Mitra)

- "Hardware Trojans and Trust in ICs,"
  - *Hot Topic Session on Hardware Security at IEEE VLSI Test Symposium,* Santa Cruz, CA, Apr '10 (Host: S. Bhunia)
- "Correlation Mining and its Applications in Reliable and Trusted Analog/RF ICs,"
  - *Rutgers University,* New Brunswick, NJ, Feb '11 (Host: K. Dana)
  - *University of Pittsburgh,* Pittsburgh, PA, Apr '10 (Host: S. Levitan)
- "Adaptive Analog Test: Feasibility and Opportunities Ahead,"
  - *Panel at IEEE VLSI Test Symposium,* Santa Cruz, CA, Apr '10 (Host: P. Nigh)
- "A Machine-Learning Approach to Analog/RF Circuit Testing,"
  - *Duke University,* Durham, NC, Dec '09 (Host: K. Chakrabarty)
  - *University of Connecticut,* Storrs, CT, Nov '09 (Host: M. Tehranipoor)
  - *Johns Hopkins University*, Baltimore, MD, Oct '09 (Host: A. Terzis)
- "Workload-Cognizant Impact Analysis and Applications in Error Detection and Tolerance in Modern Microprocessors,"
  - *Invited Talk at the International Conference on Defect and Fault Tolerance in VLSI Systems,* Chicago, IL, Oct '09 (Host: S. Tragoudas)
- "Correlation Mining and its Applications in Test Cost Reduction and Performance Calibration in Analog/RF Circuits,"
  - *IBM TJ Watson Research Center*, Yorktown Heights, NY, Aug '09 (Host: P. Kudva)
- "Challenges in Schools with Smaller EDA Programs,"
  - *Invited Talk at the Young Faculty Workshop on How to Survive and Succeed in Academia, held as part of the Design Automation Conference (DAC),* Jul '09 (Host: S. Levitan)
- "Hardware Trojan Horses: Fact or Fiction?"
  - *Pitney-Bowes*, Stamford, CT, Jun '08 (Host: B. Haas)
- "A Non-Linear Neural Classifier and its Applications in Testing Analog/RF Circuits,"
  - *Technical University of Chania*, Crete, Greece, Jul '08 (Host: A. Dollas)
  - *Jet Propulsion Lab*, Pasadena, CA, Jun '08 (Host: A. Stoica)
  - *University of Massachusetts, Amherst,* MA, May '08 (Host: S. Kundu)
  - *Cornell University,* Ithaca, NY, April '08 (Host: R. Manohar)
  - *University of Michigan,* Ann Arbor, MI, Mar '08 (Host: J. Hayes)
  - *Purdue University,* West Lafayette, IN, Mar '08 (Host: K. Roy)
  - *University of Iowa*, Iowa City, IA, Mar '08 (Host: S. Reddy)
  - *Princeton University,* Princeton, NJ, Feb '08 (Host: N. Jha)
  - *McGill University,* Montreal, Canada, Feb '08 (Host: Z. Zilic)
  - *Stanford University,* Palo Alto, CA, Feb '08 (Host: S. Mitra)
  - *Auburn University,* Auburn, AL, Feb '08 (Host: A. Singh)
  - *Georgia Institute of Technology,* Atlanta, GA, Jan '08 (Host: A. Chatterjee)
  - *University of Texas,* Austin, TX, Jan '08 (Host: D. Pan)
  - *University of Southern California,* Los Angeles, CA, Nov. '07 (Host: S. Gupta)
  - *University of California,* Santa Barbara, CA, Nov '07 (Host: L. Wang)
  - *University of Massachusetts,* Lowell, MA, May '07 (Host: M. Margala)
  - *Freescale Semiconductor*, Tempe, AZ, Oct '06 (Host: L. Luce)
  - *IBM*, Burlington, VT, Apr '06 (Host: M. Slamani)
  - *TIMA Laboratory*, Grenoble, France, Mar '06 (Host: S. Mir)
  - *Carnegie Melon University*, Pittsburgh, PA, Feb '06 (Host: S. Blanton)
  - *University of Patras*, Greece, Dec '05 (Host: D. Nikolos)
  - *Intel Corp.*, Hillsboro, OR, Dec '05 (Host: A. Meixner)
  - *Cypress Semiconductor*, Lynwood, WA, Nov '05 (Host: K. Blakkan)
  - *National Semiconductor,* San Jose, CA, Apr '05 (Host: H. Haggag)
- "Novel Reconfigurable Computing Architectures Based on Non-Volatile Nanoelectronic Devices,"
  - *Nanotechnology Research Initiative (NRI) Annual Review,* Santa Clara, CA, Nov '07 (Host: J. Wesler)
- "Statistical Analysis of Parametric Measurements and its Applications in Analog/RF Test,"
  - *Die Products Consortium (DPC),* Santa Clara, CA, Oct '07 (Host: L. Gilg)
- "Novel Reconfigurable Computing Architectures Based on Non-Volatile Ferroelectric FETs,"
  - *CRISP Review,* New Haven, CT, Sep '07 (Host: J. Tully)
- "Concurrent Error Detection in Microprocessor Controllers,"
  - *Intel Corporation,* Santa Clara, CA, May '07 (Host: A. Jas)
- "A Machine Learning Approach to the Design of Trusted Integrated Circuits,"
  - *BOEING Corp.,* Seattle, WA, Mar '07 (Host: R. Brees)
- "Testing Asynchronous Circuits: Challenges and Solutions,"
  - *Nanochronous Inc.*, Heraklion, Crete, Greece, Jul '08 (Host: C. Sotiriou)

  - *SUN Microsystems,* Menlo Park, CA, May '06 (Host: J. Ebergen)
- "A Global Optimization Framework for Soft-Error Rate Reduction in Logic Circuits,"
  - *BOEING Corp.,* Seattle, WA, Apr '06 (Host: R. Brees)
- "Implicit Functional Testing in Analog Circuits,"
  - *University of Washington,* Seattle, WA, Nov '05 (Host: S. Singh)
  - *University of California,* Los Angeles, CA, May '05 (Host: M. Ercegovac)
- "Testing Ultra-High-Speed Asynchronous Circuits,"
  - *BOEING Corp.,* Seattle, WA, May '05 (Host: W. Snapp)
- "Testing Speed-Independent Circuits,"
  - *Boston University,* Boston, MA, Dec '04 (Host: A. Taubin)
- "Concurrent Error Detection in Analog Circuits,"
  - *University of Washington,* Seattle, WA, Jan '04 (Host: M. Soma)
  - *University of Rochester,* NY, Dec '03 (Host: M. Margala)
  - *Athens Institute of Technology,* Greece, Nov '03 (Host: A. Dimitriou)
- "Concurrent Error Detection in FSMs,"
  - *Brown University,* Providence, RI, Dec '04 (Host: I. Bahar)
  - *Columbia University,* New York, NY, Nov '04 (Host: S. Nowick)
  - *University of Washington,* Seattle, WA, Jan '04 (Host: M. Soma)
  - *Rensselaer Polytechnic Institute,* Troy, NY, Dec '03 (Host: P. Drineas)
  - *Athens University of Economics and Business,* Athens, Greece, Jul '03 (Host: G. Polyzos)
  - *University of California, San Diego,* CA, May '03 (Host: A. Orailoğlu)
  - *Yale University,* New Haven, CT, Dec '02 (Host: K. Narendra)
- "Towards Cost-Effective Hierarchical Test Generation: What is Missing?,"
  - *Symbol Technologies Distinguished Lecture Series, Polytechnic University,* Brooklyn, NY, Mar '01 (Host: R. Karri)
- "Transparency-Based Testability Analysis for Hierarchical RTL Designs,"
  - *Yale University,* New Haven, CT, Apr '00 (Host: D. Henry)
  - *University of Illinois,* Urbana, IL, Apr '00 (Host: J. Patel)
  - *University of Pittsburgh,* Pittsburgh, PA, Mar '00 (Host: S. Levitan)
  - *Polytechnic University,* Brooklyn, NY, Mar '00 (Host: R. Karri)
  - *Northeastern University,* Boston, MA, Mar '00 (Host: F. Lombardi)
  - *University of California,* Irvine, CA, Feb '00 (Host: F. Kurdahi)
- "TRANSPARENT: Translation Path Analysis Rendering Test,"
  - *Intel Corp.,* Folsom, CA, Aug '99 (Host: P. Vishakantaiah)
- "ARTEMIS: Analysis of RTL Testability of Microprocessors,"
  - *Intel Corp.,* Hillsboro, OR, Dec '97 (Host: S. Davidson)

Current Post-Doctoral Associate Advisee (1):

- Dr. Angelos Antonopoulos, Ph.D. in Electrical Engineering, 2014, Technical University of Crete, Chania, Greece, Apr '15 – present
  Research Area: "Trusted and Reliable Analog/RF Integrated Circuits and Systems"

Current Ph.D. Student Advisees (13):

- Mr. Mahdi Bidmeshki, 5th year Ph.D. student in Computer Engineering
  Research Topic: "Proof-Carrying Hardware Solutions in Mixed-Signal Integrated Circuits"
- Mr. Constantinos Xanthopoulos, 5th year Ph.D. student in Computer Engineering
  Research Topic: "Applications of Spatial Correlation Extraction and Decomposition in Semiconductor Data"
- Mr. Kiruba Subramani, 5th year Ph.D. student in Electrical Engineering
  Research Topic: "Hardware Trojans in Wireless Networks"
- Mr. Monir Zamman, 5th year Ph.D. student in Computer Engineering
  Research Topic: "Cross-layer Power Conditioning in Multi-Core Mixed-Signal SoCs"
- Mr. Liwei Zhou, 5th year Ph.D. student in Computer Engineering,
  Research Topic: "Microprocessor Workload Execution Forensics"
- Mr. George Volanis, 4th year Ph.D. student in Electrical Engineering
  Research Topic: "On-Chip Intelligence for Robust and Trustworthy Analog/RF ICs"
- Mr. Yichuan Lu, 3rd year Ph.D. student in Electrical Engineering
  Research Topic: "Post-Production Performance Calibration in Analog/RF Devices"
- Mr. Gaurav Rajavendra Reddy, 3rd year Ph.D. student in Electrical Engineering

Research Topic: "Post-Layout Sensitivity Mining and its Applications in Yield Learning and Improvement"
- Ms. Christiana Kapatsori, 2nd year Ph.D. student in Electrical Engineering
  Research Topic: "Trusted Analog/Mixed-Signal ICs"
- Mr. Mustafa Shihab, 2nd year Ph.D. student in Electrical Engineering
  Research Topic: "Design Obfuscation based on a Transistor-Level Programmable Fabric"
- Mr. Yunjie Zhang, 1st year Ph.D. student in Electrical Engineering
  Research Topic: "Hardware-based Malware Detection"
- Ms. Deepika Neethirajan, 1st year Ph.D. student in Computer Engineering
  Research Topic: "Applications of Machine Learning in Semiconductor Manufacturing"
- Mr. Shiva Shankar Thiagarajan, 2nd year M.S. student in Electrical Engineering
  Research Topic: "Automotive and Autonomous Vehicle Security and Privacy"

Current M.S. Student Advisee (1):

- Mr. Christopher Rhynes, 2nd year M.S. student in Electrical Engineering
  Research Topic: "Hardware Trojans in Analog/Mixed-Signal Integrated Circuits"

Former Post-Doctoral Associate Advisee (1):

- Dr. Ke Huang, Ph.D. in Electrical Engineering, 2011, University of Grenoble, France, Feb '12 - Aug '14
  Research Area: "Applications of Statistical Learning in Testing Analog/RF Devices"
  First and Current Position: Assistant Professor, ECE Department, San Diego State University, San Diego, CA, USA

Former Ph.D. Student Advisees (10):

- Dr. Haralampos Stratigopoulos, Ph.D. in Computer Engineering, Yale University, Dec '06
  Thesis Title: "A Machine-Learning Approach to Analog/RF Circuit Testing"
  First Position: Post-Doctoral Associate, Centre National de la Recherche Scientifique (CNRS), TIMA, Grenoble, France
  Current Position: Researcher, Centre National de la Recherche Scientifique (CNRS), LIP-6, Paris, France
- Dr. Sobeeh Almukhaizim, Ph.D. in Computer Engineering, Yale University, Dec '07
  Thesis Title: "Optimization Frameworks for Designing Reliable Circuits"
  First Position: Assistant Professor, Computer Engineering Department, Kuwait University, Kuwait
  Current Position: Associate Professor, Kuwait University, Kuwait, and Director of National Center for Education Development
- Dr. Feng Shi, Ph.D. in Computer Engineering, Yale University, Dec '07
  Thesis Title: "Fault Simulation and Test Generation Strategies for Asynchronous Circuits"
  First Position: Senior Electrical Engineer, Skyworks Solutions, Irvine, CA, USA
  Current Position: Mixed-Signal/RF Circuit Designer, Marvell Semiconductor, Irvine, CA, USA
- Dr. Naghmeh Karimi, Ph.D. in Computer Engineering, University of Tehran, Iran, Nov'09 (visiting 7/07 - 6/09)
  (Co-Advised with Dr. Zain Navabi)
  Thesis Title: "Concurrent Error Detection in Microprocessor Controllers"
  First Position: Post-doctoral Researcher, Duke University, Durham, NC, USA
  Current Position: Assistant Professor, University of Maryland Baltimore County, Baltimore, MD, USA
- Dr. Nathan Kupp, Ph.D. in Computer Engineering, Yale University, Dec '12
  (2012 E.J. McCluskey Best Doctoral Thesis Award and Recipient of SRC Graduate Fellowship)
  Thesis Title: "Integrated Optimization of Semiconductor Manufacturing: A Machine Learning Approach"
  First Position: Statistical Power Optimization Researcher, Apple Inc., Cupertino, CA, USA
  Current Position: Lead Data Scientist, Thumbtack, San Francisco, CA, USA
- Dr. Michail Maniatakos, Ph.D. in Computer Engineering, Yale University, Dec '12
  Thesis Title: Workload-cognizant, Cross-layer Impact Analysis to Enhance Resiliency in Modern Microprocessors
  First & Current Position: Assistant Professor, Electrical and Computer Engineering Department, New York University, Abu Dhabi, UAE
- Dr. Yier Jin, Ph.D. in Computer Engineering, Yale University, Dec '12
  Thesis Title: Trusted Integrated Circuits
  First Position: Assistant Professor, Electrical Engineering and Computer Science Department, University of Central Florida, Orlando, FL, USA
  Current Position: Associate Professor and Endowed IoT Term Professor, Electrical and Computer Engineering Department, University of Florida, Gainesville, FL, USA
- Mr. Dzmitry Maliuk, Ph.D. in Computer Engineering, Yale University, Dec '13
  Thesis Title: "On-Chip Neural Network Design for Built-in Self-Test of Analog/RF Circuits"

First & Current Position: Analyst, Quantlabs, Houston, TX, USA

- Dr. Yu Liu, Ph.D. in Electrical Engineering, University of Texas at Dallas, May '17
  Thesis Title: "Hardware Trojans in Wireless Cryptographic ICs"
  First and Current Position: Research Staff Member, Samsung Research, Plano, TX
- Dr. Ali Ahmadi, Ph.D. in Computer Engineering, University of Texas at Dallas, May '17
  Thesis Title: "Applications of Machine Learning in Test Cost Reduction, Yield Estimation and Fab-of-Origin Attestation of Integrated Circuits"
  First and Current Position: Member of Technical Staff, GlobalFoundries, Malta, NY

Former M.S. Student Advisees (5):

- Mr. Thomas Verdel, M.S. in Computer Engineering, Dec '02 (Yale University)
  Research Topic: "Concurrent Error Detection in Asynchronous Circuits"
  Current Position: Quantitative Portfolio Manager, AXIA Investment Management, Tulsa, OK, USA
- Mr. He Huang, M.S. in Computer Engineering, Dec '09 (Yale University)
  Research Topic: "Design & Silicon Implementation of a Self-Healable LNA"
  Current Position: Analog/RF Design Engineer, Broadcom, Sunnyvale, CA, USA
- Mr. Yichuan Lu, M.S. in Electrical Engineering, May '14 (University of Texas at Dallas)
  Research Topic: "Post-Production Performance Calibration in Analog/RF Devices"
  Current Position: Ph.D. Student, TRELA Lab, University of Texas at Dallas, USA
- Mr. Tianyu Chen, M.S. in Electrical Engineering, May '14 (University of Texas at Dallas)
  Research Topic: "Implementation of OpenSPARC on an FPGA Emulation Platform for Forensics Analysis"
  Current Position: Test Engineer, Foxconn, Houston, TX, USA
- Mr. Gaurav Rajavendra Reddy, M.S. in Electrical Engineering, May '17 (University of Texas at Dallas)
  Research Topic: "A Routing Methodology for a Novel CMOS Transistor-level Reconfigurable Array"
  Current Position: Ph.D. Student, TRELA Lab, University of Texas at Dallas, USA

Ph.D. and/or Research Committee Participation:

- Dr. Meisam Roshan, Ph.D. in Electrical Engineering, University of Texas at Dallas (Advisor: C. Sechen)
- Dr. Akshay Sridharan, Ph.D. in Electrical Engineering, University of Texas at Dallas (Advisor: C. Sechen)
- Dr. Yanghun Yun, Ph.D. in Electrical Engineering, University of Texas at Dallas (Advisor K. O)
- Dr. Yongtao Geng, Ph.D. in Electrical Engineering, University of Texas at Dallas (Advisor: D. Ma)
- Dr. Yuan Zhou, Ph.D. in Electrical Engineering, University of Texas at Dallas (Advisor: Y. Chiu)
- Dr. Zhao Wang, Ph.D. in Electrical Engineering, University of Texas at Dallas (Advisor: C. Sechen)
- Dr. Yi Zhang, Ph.D. in Electrical Engineering, University of Texas at Dallas (Advisor: D. Ma)
- Dr. Zhengming Fu, Ph.D. in Computer Engineering, Yale University (Advisors: A. Savvides, E. Culurciello)
- Dr. Dimitrios Lymberopoulos, Ph.D. in Computer Engineering, Yale University (Advisor: A. Savvides)
- Dr. Deakwoo Jung, Ph.D. in Computer Engineering, Yale University (Advisor: A. Savvides)
- Dr. Athanasios Bamis, Ph.D. in Computer Engineering, Yale University (Advisor: A. Savvides)
- Dr. Thiago Teixeira, Ph.D. in Computer Engineering, Yale University (Advisor: A. Savvides)
- Dr. Evan Park, Ph.D. in Computer Engineering, Yale University (Advisor: E. Culurciello)
- Dr. Melinda Agyekum, Ph.D. in Computer Science, Columbia University (Advisor: S. Nowick)

M.S. Thesis Committee Participation:

- Mr. Xiao He, M.S. student in Electrical Engineering, University of Texas at Dallas (Advisor: C. Sechen)

Teaching Experience:

- The University of Texas at Dallas, Richardson, TX, USA, Jul '11 – Present
  Instructor for Courses:
  - EE/CE/TE 1202 (Spring '12, Spring '13, Spring '14, Spring '15, Spring '16, Spring '17): *"Introduction to Electrical Engineering II"*
  - EE/CE/CS 6304 (Spring '12, Fall '12, Fall '13, Fall '14, Fall '15, Fall '16, Fall '17): *"Computer Architecture"*
  - CE 7V80 (Spring '13, Spring '14, Spring '15, Spring '16): *"Special Topics: Trusted and Secure Integrated Circuits & Systems"*
  - EE 7V81 (Spring '17): *"Special Topics: Applications of Machine Learning in Semiconductor Manufacturing"*
- Yale University, New Haven, CT, USA, Jan '01 – Jun '11
  Instructor for Courses:
  - EENG 201b (Spring '06, Spring '07, Spring '08, Spring '10, Spring '11): *"Introduction to Computer Engineering"*

  - EENG 201a (Fall '03): *"Perspectives in EE: Semiconductors, Computers, and Communications"*
  - EENG 348a (Fall '01, Fall '02, Fall '03, Fall '04): *"Digital Systems"*
  - EENG 462b (Spring '02, Spring '03, Spring '06, Spring '07): *"Digital System Testing and Design for Testability"*
  - ENAS 921a (Fall'10): *"Advanced Topics in Computer Engineering"*
- University of California San Diego, CA, USA, Computer Science & Engineering Department, Jan '96 - Jun '01
  Teaching Assistant for Courses: *"Discrete Mathematics", "Advanced Computer Architecture", "CAD for VLSI"*
- University of Patras, Greece, Computer Engineering & Informatics Department, Sep '94 - Jun '95
  Teaching Assistant for Courses: *"VLSI Design & Lab", "Digital Logic Design & Lab"*

Teaching Fellow / Teaching Assistant Advisees:

- Mr. Monir Zaman, EE/CE/CS 6304, Fall '16, Fall '17, EE/CE/TE 1202, Spring '17
- Mr. Mahdi Bidmeshki, EE/CE/TE 1202, Spring '16
- Mr. Gaurav Rajavendra Reddy, EE/CE 7V80, Spring '16
- Mr. Constantinos Xanthopoulos, EE/CE/CS 6304, Fall '15, Spring '17
- Mr. Liwei Zhou, EE/CE/CS 6304, Fall '14, EE/CE 7V80, Spring '15
- Mr. Tianyu Chen, EE/CE/TE 1202, Spring '14
- Mr. Yongtao Geng, EE/CE/TE 1202, Spring '14
- Mr. Tianyu Chen, EE/CE/CS 6304, Fall '13
- Mr. Meisam Roshan, EE/CE/TE 1202, Spring '13
- Mr. Jaewook Lee, EE/CE/TE 1202, Spring '13
- Mr. Masood Farshbaf Zinati, EE/CE 6304, Fall '12
- Mr. Nanxian Li, EE/CE/TE 1202, Spring '12
- Mr. Mihael Klausing, EE/CE/TE 1202, Spring '12
- Mr. Rasoul Yousefi, EE/CE 6304, Spring '12
- Mr. Yier Jin, EENG201b Laboratory, Spring '10
- Mr. Dzmitry Maliuk, EENG201b Laboratory, Spring '11
- Mr. Michail Maniatakos, EENG201b Laboratory, Spring '10, Spring '11
- Mr. Evan Park, EENG201b Laboratory, Spring '08
- Mr. Thiago Teixeira, EENG201b Laboratory, Spring '07, Spring '08
- Mr. Zhengming Fu, EENG201a Laboratory, Fall '03, EENG201b Laboratory, Spring '06, Spring '07
- Mr. Sobeeh Almukhaizim, EENG348a/CPSC338a Laboratory, Fall '03, EENG462b/EENG507b, Spring '06, Spring '07
- Mr. Yu Chen, EENG348a/CPSC338a Laboratory, Fall '04
- Mr. Haralampos Stratigopoulos, EENG462b/EENG507b, Spring '03
- Ms. Yanning Sun, EENG348a/CPSC338a Course, Fall '01, Fall '02, Fall '03
- Mr. Thomas Verdel, EENG348a/CPSC338a Laboratory, Fall '02
- Mr. Fanshi Zhao, EENG348a/CPSC338a Laboratory, Fall '01

Senior Project Advisees (at Yale University):

- Mr. Eric Love, Spring '11 **(TIFS Paper Published in 2011)**
  Topic: "Proof Carrying Hardware Intellectual Property"
- Mr. James Dardig, Spring '08 **(VTS Paper Published in 2008)**
  Title: "Machine Learning-Based Nanoscale Architectures"
- Mr. John Kearny, Spring '07
  Title: "Mixed-Signal Test Methods on a Cypress PSOC Device"
- Mr. Sam Evers, Spring '05
  Title: "A Floating-Gate CMOS Analog Artificial Neural Network"
- Ms. Amy Wong, Spring '04
  Title: "Selection of Measurements in Analog Circuit Test: Implementing an Adaptive Floating Search Method in C++"
- Ms. Melis Kahya, Spring '04
  Title: "Oscillation Test with Amplitude Considerations"
- Mr. Abraham Tarapani, Spring '04
  Title: "Design and Implementation of an Advanced Toy Processor on an FPGA"
- Mr. Konstantinos Rokas, Spring '03 **(Awarded Franz Tuteur Prize)**
  Title: "Low-Cost Concurrent Error Detection in FSMs using Convolutional Codes" **(DFTS Paper Published in 2004)**
- Mr. Andrew Barton-Sweeney, Spring '02 (co-advised with Prof. Yang-Richard Yang)
  Title: "IP UDP FPGA Hardware Design"

Undergraduate Research Advisees (at University of Texas at Dallas):

- Ms. Usuma Thet, Summer '14 (**Supported by NSF REU**)
  Topic: "Visualization of FPGA-Emulated OpenSPARC T1 Workload Execution Traces"
  Current Position: Senior, Computer Science Department, University of Texas at Dallas

Former Visiting Undergraduate Research Advisees (at University of Texas at Dallas):

- Mr. Themistoklis Melissaris, Spring '14
  Topic: "Instrumentation of FPGA-Emulated OpenSPARC T1 for Workload Execution Tracing"
  Current Position: Ph.D. student, Electrical Engineering Department, Princeton University

Undergraduate Research Advisees (at Yale University):

- Mr. Eric Love, Summer '10 (**Supported by NSF REU**) **(HOST Paper Published in 2011)**
  Topic: "Proof Carrying Hardware"
- Mr. Ross Feinstein, Summer '09 (**Supported by NSF REU**)
  Topic: "Concurrent Error Detection in Modern Microprocessors"
- Mr. Kyle Gong, Summer '08 (**Supported by Intel Gift**)
  Topic: "Synthesis for Reliability using SPFDs"
- Mr. Eric Love, Summer '08 (**Supported by NSF REU**) **(TVLSI Paper Published in 2009)**
  Topic: "Soft-Error Tolerant Gate Decomposition in Asynchronous Burst Mode Machines"
- Mr. James Dardig, Summer '07 (**Supported by NSF REU**) **(VTS Paper Published in 2008)**
  Topic: "Machine Learning-Based Nanoscale Architectures"
- Mr. Sam Evers, Fall '04 and Summer '04 **(Awarded Dean's Fellowship)**
  Topic: "Feature Selection Algorithms for Classification-Based Analog Circuit Testing"
- Mr. Xin Tong, Summer '04 **(Supported by Paul Moore Award)**
  Topic: "Implementation of an Educational Toy Processor on the Pegasus FPGA Board"
- Mr. Nitin Gupta, Spring '04
  Topic: "In-Depth Analysis of the Compaction of Sequential Test Sequences"
- Mr. Travis Penn, Fall '03 and Summer '03
  Topic: "Test Response Compaction"
- Mr. Emmanuel Imbeah, Summer '03 **(Supported by Paul Moore Award)**
  Topic: "Design of an Educational Toy Processor"
- Mr. Konstantinos Rokas, Fall '02 **(Awarded Franz Tuteur Prize) (DFTS Paper Published in 2004)**
  Topic: "Concurrent Error Detection with Latency in Finite State Machines"
- Mr. Raul Ruiz, Spring '02 and Fall '01 **(Supported by Paul Moore Award)**
  Topic: "Concurrent Test Methods for Combinational Circuits"

Institutional and Departmental Service (at University of Texas at Dallas):

- Member of the University-Wide Committee on Academic Qualifications (Fall '16, Spring'17, Fall '17, Spring'18)
  Junior Faculty Mentor, Electrical and Computer Engineering Department (Fall '17, Spring '18)
- Committee on Academic Affairs, Member, Jonsson School of Engineering and Computer Science (Fall '14, Spring '15)
- Committee on Space Allocation, Member, Jonsson School of Engineering and Computer Science (Fall '14, Spring '15)
- Doctoral Qualifying Exam Committee in Digital Systems, Member (Fall '14, Spring '15)
- Faculty Search Committee in Electrical Engineering, Member (Spring '14, Spring '15, Fall '15, Spring '16, Fall '16, Spring '17)
- Doctoral Qualifying Exam Committee in Digital Signal Processing, Member (Spring '14)
- Doctoral Qualifying Exam Committee in RF ICs, Member (Fall '13)
- Faculty Search Committee in Electrical Engineering, Chair (Fall '12 - Spring '13)
- Doctoral Qualifying Exam Committee in Computer Engineering, Member (Spring '13)
- Doctoral Qualifying Exam Committee in VLSI, Chair (Fall '12)
- Faculty Search Committee in Computer Engineering, Member (Spring '12)
- Graduate Admissions Committee in Computer Engineering, Member (Fall '11, Spring'12, Fall '12, Spring '13, Fall '13, Spring '14)
- TxACE IT Specialist Search Committee, Chair (Fall '11)
- Doctoral Qualifying Exam Committee in Computer Engineering, Chair (Fall '11)

Institutional and Departmental Service (at Yale University):

- Director of Undergraduate Studies in Electrical Engineering (Fall '07 - Spring '08)
- Course of Study Committee, Member (Spring '06 - Spring '07)
- Computer Engineering Seminar, Founder (Fall '04)
- Curriculum Committee, Member (Fall '02 - Spring '04)
- Graduate Math Requirement Committee, Member (Spring '03)
- Graduate Admissions Committee, Member (Spring '01 - Spring '03, Spring '07)
- Computer Engineering Faculty Search Committee, Member (Fall '02 - Spring '04)

Professional Service:

- Associate Editor:
  - *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (T.CAD), 2018 - present*
  - *IEEE Transactions on Information Forensics and Security (T.IFS), 2015 - present*
  - *IEEE Design & Test of Computers (D&T), 2015 - present*
  - *Springer Journal of Electronic Testing: Theory and Applications (JETTA), 2015 - present*
- Guest co-Editor:
  - *IEEE Transactions on Computers (T.COMP), Special Section on Chips and Architectures for Emerging Technologies (04/2011)* (with A. Benso and P. Mazumder)
  - *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (T.CAD), Special Issue on Hardware Security and Trust (06/15)* (with R. Karri, F. Koushanfar, S. Bhunia, M. Potkonjak, A. Sadeghi and O. Sinanoglu
- General Chair:
  - *IEEE VLSI Test Symposium (VTS'16 - '17)*
- Vice General Chair:
  - *IEEE VLSI Test Symposium (VTS'15)*
  - *IEEE International On-Line Testing Symposium (IOLTS '15)*
- Program Chair:
  - *Texas Analog Center of Excellence Symposium (TxACE'15)*
  - *IEEE VLSI Test Symposium (VTS'13 - '14)*
  - *IEEE Computer Society, Test Technology Technical Council, Test Technology Education Program (TTEP'10 -'12)*
- Session Chair:
  - *NSF Foundations of Secure and Trusted Hardware Workshop (FOSTER'17)*
  - *IEEE International Workshop on Hardware Oriented Security and Trust (HOST'13)*
  - *IEEE Design Automation and Test in Europe (DATE '13 - '14, '17)*
  - *IEEE European Test Symposium (ETS'08, '17)*
  - *IEEE International Test Conference (ITC'03 -'04, '06 -'08, '12, '16)*
  - *IEEE International Conference on Computer Aided Design (ICCAD'07, '09, '16)*
  - *IEEE VLSI Test Symposium (VTS'03 -'08, '15)*
  - *IEEE North Atlantic Test Workshop (NATW'02)*
- Organizing Committee Member:
  - *IEEE International Test Conference (ITC'17) - Area Topic Coordinator for Analog and RF Test"*
  - *IEEE International Test Conference (ITC'12 - '13) – Area Topic Coordinator for "Product Test (t<0 and t>0)"*
  - *IEEE VLSI Test Symposium (VTS'11 - '12) – Registration Chair*
  - *IEEE VLSI Test Symposium (VTS'09 - '10) – Publications Chair*
  - *IEEE International Conference on Computer Design (ICCD'12) –Track Co-Chair, Test, Verification and Security*
  - *IEEE International On-Line Testing Symposium (IOLTS '12 - '14) – Vice Program Co-Chair*
  - *IEEE International On-Line Testing Symposium (IOLTS'10 - '11) – Special Sessions Co-Chair*
  - *IEEE International On-Line Testing Symposium (IOLTS'08 - '09) – Publicity Chair*
  - *IEEE International Workshop on Hardware Oriented Security and Trust (HOST'12) – Panel Chair*
  - *IEEE International Workshop on Hardware Oriented Security and Trust (HOST'08) – Finance Chair*
  - *IEEE International Workshop on Design for Reliability and Verifiability (DRV'08 - '09, '11) – Publicity Chair*
  - *IEEE International Workshop on Test/Validation of High-Speed Analog Circuits (TVHSAC'09-'10) – Publicity Chair*
- Technical Program Committee Member:
  - *IEEE International Test Conference (ITC'11 - '17)*
  - *IEEE/ACM Design Automation Conference (DAC'12 - '14, '18)*
  - *TxACE Symposium (TxACE '12)*
  - *IEEE International Conference on Computer-Aided Design (ICCAD '09 -'11, '15-'17)*
  - *IEEE VLSI Test Symposium (VTS'08 -'18)*

  - *IEEE Design Automation and Test in Europe (DATE'07 -'11, '13-'15, '18)*
  - *IEEE Symposium on Defect and Fault Tolerance in VLSI Systems (DFTS'08 -'10, '12-'13)*
  - *IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC'07, '09-'10)*
  - *IEEE On-Line Testing Symposium (IOLTS'05 -'18)*
  - *ACM Great Lakes Symposium on VLSI (GLSVLSI'04 - '05, '09 -'10)*
  - *IEEE European Test Symposium (ETS'04 -'18)*
  - *IEEE International Symposium on Hardware Oriented Security and Trust (HOST'08-'18)*
  - *IEEE International Workshop on Test/Validation of High-Speed Analog Circuits (TVHSAC'13-'15)*
  - *Workshop on Cryptographic Hardware and Embedded Systems (CHES'12)*
  - *IEEE International Mixed-Signals, Sensors, and Systems Test Workshop (IMS3TW'11-'17)*
  - *IEEE Microprocessor Test and Verification Workshop (MTV'10-'13)*
  - *IEEE European Test Workshop (ETW'02 -'03)*
  - *IEEE Wireless Test Workshop (WTW'08 - '10)*
  - *IEEE North Atlantic Test Workshop (NATW'03 - '10)*
  - *IEEE International Workshop on Reliability Aware System Design and Test (RASDAT'10 -'12)*
  - *IEEE International Conference on Automation, Quality & Testing, Robotics (AQTR'05 -'06)*
- Electronic Broadcasting Editor:
  - *IEEE Computer Society, Test Technology Technical Council, Communications Group (EBS '04 -'08)*
- Vice-Chair:
  - *IEEE Computer Society, Test Technology Technical Council, Technical Meetings Group (TMG '09)*
  - *IEEE Computer Society, Test Technology Technical Council, Tutorials and Education Group (TTEP '10 - '12)*
- Publicity Co-Chair:
  - *IEEE Computer Society, Test Technology Technical Council, Tutorials and Education Group (TTEP '04 -'09)*
- Panelist:
  - *National Science Foundation (NSF), May '04, Sep '08, Oct '09, Nov '11, Feb '12, Jun '14, Apr '15, Mar '16, Apr '16, Nov '17*
- Technical Referee:
  - *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD)*
  - *IEEE Transactions on Computers (TCOMP)*
  - *IEEE Transactions on VLSI (TVLSI)*
  - *IEEE Transactions on Information Forensics and Security (TIFS)*
  - *IEEE Transactions on Circuits and Systems (TCAS-II)*
  - *IEEE Transactions on Instrumentation and Measurement (TIM)*
  - *IEEE Transactions on Reliability (TREL)*
  - *IEEE Transactions on Mobile Computing (TMC)*
  - *IEEE Transactions on Dependable and Secure Computing (TDSC)*
  - *IEEE Design & Test of Computers Magazine (D&T)*
  - *IEEE Communications Magazine (COM)*
  - *Springer Journal of Electronic Testing (JETTA) (formerly published by Kluwer)*
  - *Springer Journal of Cryptographic Engineering (JCEN)*
  - *IEEE International Test Conference (ITC)*
  - *IEEE VLSI Test Symposium (VTS)*
  - *IEEE Design Automation Conference (DAC)*
  - *IEEE Design Automation and Test in Europe (DATE)*
  - *IEEE International Conference on Computer-Aided Design (ICCAD)*
  - *IEEE International Conference on Computer Design (ICCD)*
  - *IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC)*
  - *IEEE International Symposium on Circuits and Systems (ISCAS)*
  - *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFTS)*
  - *IEEE On-Line Testing Symposium (IOLTS)*

Volunteering Activities:

- Sports Information Assistant, Athens 2004 Olympic Games, Aug '04
- Faculty Mentor, Hellenic Student Association, Yale University, (HSA '01-'10)
- Local Arrangements Advisor, Team Lux Participation in Phaethon Solar Car Race, Athens, Greece, May '04

Professional Associations:

- IEEE Senior Member, Test Technology Technical Council, Technical Chamber of Greece