Post-Production Calibration of Analog/RF ICs: Recent Developments and A Fully Integrated Solution

Angelos Antonopoulos, Georgios Volanis, Yichuan Lu and Yiorgos Makris
Department of Electrical and Computer Engineering, The University of Texas at Dallas, Richardson, TX 75080
Email: {aanton, Georgios.Volanis, yichuan5, yiorgos.makris}@utdallas.edu

Abstract—**We present recent developments on post-production calibration of analog and radio frequency (RF) integrated circuits (ICs) mainly focusing on on-chip solutions. Specifically, we summarize the state-of-the-art on both direct and statistical calibration techniques. The latter typically employ on-die sensors, which estimate the circuit under test (CUT) performances and tuning knobs, which along with machine learning-based methods are capable of calibrating the CUT. Existing sensors, tuning knobs and machine learning-based implementations are discussed and their limitations are outlined. Lastly, a fully integrated new architecture for on-chip calibration of a low-noise amplifier (LNA) through the use of an analog neural network is introduced.**

I. Introduction

ICs are typically designed to operate within a specific range of acceptable performances which is dictated by the application and the standard they need to comply. However, when deployed in the field, ICs are likely to be impacted by several factors which either move their performances outside the accepted range or shift their operating point to a non-ideal yet acceptable value, thus, resulting in yield loss and reduced performance, respectively. While environmental conditions and aging play an important role for this undesired behavior, process variations constitute the fundamental factor for performance shifts and yield loss. The problem becomes more serious as technology scales down to the decananometer regime, wherein process variations become a non-negligible percentage of the transistor size. Analog/RF ICs exploit the downscaling of the semiconductor processes to achieve higher unity gain frequencies, which correspondingly improves certain device characteristics. However, at the same time, analog and RF ICs are highly affected by process variations, which may deteriorate their performances. Typically, analog/RF designers will follow conservative approaches in order to achieve moderate rather than extreme (close to the edge of specifications) circuit performances. However, such conservative approaches may significantly degrade output characteristics. Hence, more drastic techniques are needed to counteract the effect of process variations in analog/RF ICs and fine tune their operating point in order to improve their output characteristics and recover yield.

To this end, post production calibration techniques have been introduced, which can be generally categorized as off-chip and on-chip. The former are performed during production test whereas in the latter the calibration mechanism is integrated on-die. Further on, based on whether performances of the analog/RF IC are measured directly or indirectly via statistically correlating low-cost measurements, i.e. alternate tests with performances, existing on-chip calibration methods can be sub-categorized to direct and statistical methods. Statistical methods employ three entities[1] to achieve the desired results: (a) sensors, which monitor all types of circuit variations, (b) tuning knobs, which adjust circuit performances, and (c) machine learning algorithms which build a model given the tuning knob settings and their corresponding sensor measurements and accordingly select a tuning knob setting which optimizes certain performances of the CUT. Sensors are split to intrusive and non-intrusive depending on whether they are connected to the CUT. Tuning knobs may be found as ideal power sources as well as passive and active components. Finally, machine learning-based algorithms can be categorized into software solutions and hardware implementations. A taxonomy of post-production calibration methods is summarized in Figure 1.
The rest of this paper is structured as follows: Section II presents recent developments on both off-chip and on-chip post-fabrication calibration and elaborates on direct and statistical methods. Section III outlines the state-of-the-art on sensors, tuning knobs as well as implementations of machine learning blocks. Their characteristics and limitations are pointed out. Finally, in Section IV, a fully integrated solution employing an analog neural network for self-test and self-tune is introduced.

II. Off- and On-chip Solutions

As discussed in [1]–[3], several implementations of calibration methods during production test have been proposed in the literature. The most lengthy in time is based on iterative test and tune using external automatic test equipment (ATE), wherein performance testing is repeated for every knob setting until all desired performances are reached. A time-wise improvement of the iterative test and tune method relies on alternate (low-cost) tests in which multiple performances are inferred from simple measurements [1]. To further reduce test time, one-shot approaches can be used [4]. One-shot calibration methods rely on a set of low-cost measurements

[1]We note that off-chip solutions may also comprise these three entities [1].

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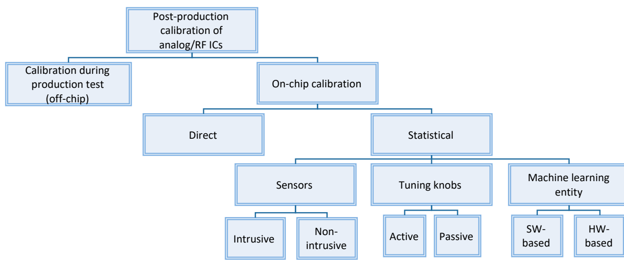

Fig. 1: Taxonomy of post-production calibration techniques.

obtained for a single setting of the tuning knobs, and employ statistical learning in order to train models which are used for selecting a final knob position based on the low-cost measurements. Yet, the trained model is external to the CUT as shown in Figure 2(a). Off-chip calibration methods do not impose significant overhead since the machine-learning block (if any) is implemented off-chip. However, they experience certain limitations, since the CUT needs to periodically interact with off-chip components. On-chip calibration methods on the other hand, offer an alternative which addresses this limitation by integrating all required components on the same die with the CUT [5]–[8], as shown in Figure 2(b). The trained model can be implemented in software using for example a digital signal processor (DSP), as depicted in Figure 2(b), or using a hardware implementation [5]. On-chip integration of the required hardware imposes a significant area overhead. However, it not only reduces reliance on expensive ATE but also facilitates periodic adaptation to operating conditions, aging, and wear-&-tear [5].

A. Direct Methods

Direct methods typically employ various probe points in the chip which directly sample the performance of the CUT [6]. For example in [7], the frequency of a voltage controlled oscillator (VCO) is measured by a frequency-to-digital converter, whereas its phase noise is estimated by the current of the VCO's tail transistor. Accordingly, tuning knobs are used to compensate for shifts in the VCO's frequency characteristics. A similar approach, which enables measurement of the gain and phase mismatch of an RF phased array for in field calibration, was recently presented in [9]. Using such a perspective though, a limited number of output characteristics can be improved. This drawback can be overcome by using an on-chip optimization engine which facilitates simultaneous tuning for multiple CUT characteristics. Specifically in [6], a built-in-self-test (BIST) measures the response of the analog CUT under excitation in the time or frequency domain and accordingly the transfer function of the CUT is calculated. Based on the difference between the estimated and target transfer function, multiple CUT performances are optimized using a fully-digitized optimization engine.

B. Statistical Methods

In order to enable a more flexible and adaptable calibration method, statistical techniques, which replace direct performance measurements with low-cost sensors, have been recently presented [5]. Machine learning-based techniques are used to build a correlation model between the indirect low-cost sensor measurements and the circuit performances and accordingly to predict the knob position which optimizes performance of the CUT solely based on the indirect low-cost measurements [2]. As discussed in [6], statistical methods suffer from two limitations: (i) limited accuracy between predicted and actual characteristics and (ii) difficulties in integrating the statistical model on-chip. However, recent developments have shown that both limitations can be addressed. In [5] the analog neural network which provides the required intelligence for on-die learning achieves a very low power overhead while simultaneously being able to predict the optimal knob setting which maximizes the overall CUT performance. Specifically, out of the 64 CUT (LNA in this case) instances that we tested, 61 were tuned to the knob setting providing the best performance, whereas the remaining 3 were tuned to the setting with the second best performance. Yet, the average percentile overall performance difference when the second best setting is chosen is negligible.

III. Sensors, Tuning Knobs and Machine-Learning Implementations

A. Sensors

Alternate tests can be either based on intrusive sensors, i.e. sensors which are electrically connected to the CUT or non-intrusive, transparent sensors, which do not have any electrical connection to the CUT. Intrusive sensors can be found in the form of current as well as envelope detectors [10] and peak detectors [5], which provide a DC output equivalent to the peak value of the transient signal. On the other hand, non-intrusive sensors are inspired by the process control monitors, which are used to monitor technology specific parameters on a wafer [1] and can have a wide range of implementations based on the CUT topology. For example, in [11], wherein the CUT is a three-stage 60GHz LNA, non-intrusive sensors are chosen as active common-source and cascode configurations as well as passive structures, such as capacitors, resistors and micro-strip transmission lines. By placing these non-intrusive sensors close to CUT, it is likely that the process variations affecting the CUT will be adequately captured, i.e. the CUT performances will be strongly correlated to the measurements of these non-intrusive sensors.

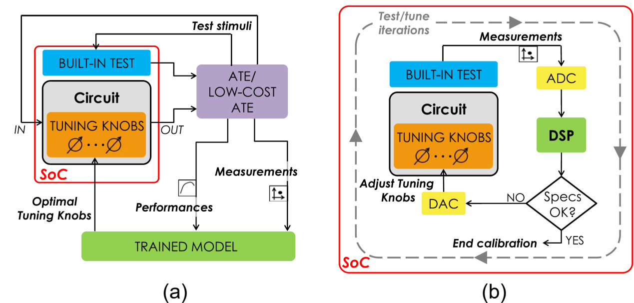

Fig. 2: Calibration (a) during testing, (b) after deployment [1].

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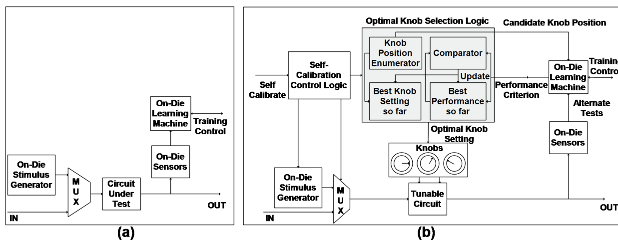

Fig. 3: Proposed (a) self-test and (b) self-calibration method.

B. Tuning Knobs

Tuning knobs are an integral part of the calibration process and operate on the design parameters of the IC, e.g., bias voltages and currents. In [12], tuning knobs are considered as ideal supply sources. Practical implementations of tuning knobs have been proposed in the literature, mainly in the form of tunable MOS capacitors, current sources, transistors with programmable width, adjustable inductors, bias actuators, and transmission lines [7], [8], [13]. Reported results verify that tuning knobs can adjust performances of RF ICs, such as power amplifiers and LNAs, and recover yield under excessive process variations. Nevertheless, tuning knobs are also subject to process variations and, thus, their impact on tuning effectiveness has to be considered. The problem arises when multiple instances of the knob circuitry are not available during derivation of the training dataset. In such a case, training is performed with ideal knob values, i.e. not affected by process variations whereas testing is performed with real values, i.e. affected by process variations. To account for such external knob non-idealities and the corresponding higher calibration error, the existing knob data can be synthetically enriched by Monte Carlo simulations to account for the impact of knob process variations on the performances and alternate tests [14].

C. Machine-Learning Implementations

The intelligence provided by the machine learning algorithm which is used for selecting the best knob setting is typically implemented in software, running either on an external computer or on an on-chip DSP [12]. While this implementation provides accurate results, its power overhead is inherently high. An alternative solution could be to use an on-chip digital neural network. However, not only its power and area overhead would be prohibitive but also additional analog-to-digital converters (ADC) and digital-to-analog converters (DAC) would be required to translate the signals between the analog CUT space and the digital neural network space. A hardware realization of an on-die analog neural network implementing a regression function was firstly introduced in [5], [15]. The analog neural network is trained to predict a Figure of Merit (FoM) reflecting the overall performance of the CUT, based on a single set of low-cost alternate tests provided by on-chip sensors in response to an on-chip generated stimulus. The intelligent entity (analog neural network) and CUT (LNA) have been implemented on two different boards, using 0.35um and 130nm CMOS processes respectively and interact externally. The results from the two boards show that the analog neural network is capable of efficiently calibrating the LNA. Despite the very promising results, this work was mainly used as a proof of concept since the intelligence entity and the CUT were implemented on separate chips.

IV. A Fully Integrated On-Chip Solution

To address most of the limitations summarized in the previous Sections and verify the proof-of-concept presented in [5], [15], we introduce a statistical method for self-test and self-calibration, wherein the intelligent entity is integrated on the same chip with the CUT.

As depicted in Figure 3, the proposed self-test and self-calibration method requires the integration of measurement sensors, a stimulus generator, and an on-die learning machine alongside the CUT. During self-test/tune, the stimulus generator is connected to the CUT, and outputs a set of test signals to initiate the test/tune process. A set of sensors capture the responses of the CUT to the applied test signals, and passes them to the learning machine entity which will perform the desired actions. For self-test, the process is described in Figure 3(a). The on-die learning machine is trained to perform the task of classification by using the output of measurement sensors. Essentially, the learning entity will make a pass/fail decision based on the responses of the CUT to the test signals produced by a stimulus generator. As depicted in Figure 3(b), for self-calibration along with tuning knobs, whose various settings are capable of varying the performances of the circuit, permanent storage for their selected values, is also included. In addition, an on-die learning machine, implementing a regression function which will be trained to predict the value of an optimization criterion, based on the values produced by the sensors in response to the generated stimulus, is required. Additional simple logic for controlling the self-calibration process, as well as selecting the optimal knob position based on the predicted optimization criterion completes the proposed architecture.

The knob tuning process is shown in Figure 4. It starts with the self-calibration control logic activating the stimulus generator and the measurement sensors, in order to collect the required alternate tests. We emphasize that, in line with the previously proposed one-shot calibration methods [4], only one set of alternate tests is required for predicting the optimization criterion for all positions of the knobs. Once

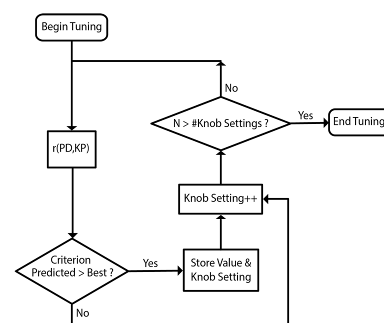

Fig. 4: Knob tuning process.

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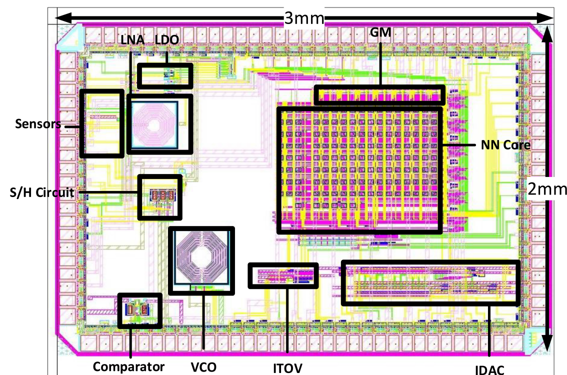

Fig. 5: Layout of fabricated die.

the alternate tests are collected, the self-calibration control logic cycles through all possible knob settings, one at a time. Each knob setting is provided along with the saved alternate tests to the trained on-die learning machine, which predicts the corresponding value of the performance criterion. A comparator is then used to evaluate whether this value is better than the best value seen so far during the tuning process. In case it is, it replaces the stored best value and the corresponding best knob setting seen so far is also updated. Otherwise, the controller proceeds to the next knob setting and the process repeats until all knob settings have been considered. At the end of this process, the best knob setting is used to calibrate the tunable circuit.

Training of the on-die learning machine is performed similarly to [5], i.e. a training dataset is produced based on measurements from multiple CUT instances, for all possible knob positions and for all desired performances along with the corresponding sensor measurements. We emphasize that along with self-test and self-calibration, the proposed architecture can be reused for on-line test, collecting diagnostics, etc.

The proposed architecture includes a tunable LNA, both intrusive (peak detector) and non-intrusive (simple transistors) sensors, a VCO, which serves as an on-die stimulus generator, three low-dropout regulators (LDOs) [14], which act as the tuning knobs biasing the LNA, five unity-gain high precision sample and hold (S/H) circuits, and a custom-designed analog neural network (NN core).The neural network peripheral circuits that provide support for fast programming and interfacing with the external world, i.e. a differential transconductor (GM), a current-to-voltage converter (ITOV), and a digitally controlled current source (IDAC) are also integrated on-die. The NN core operates below threshold, achieving sub-μW power consumption and incorporates floating gate transistors for long-term retention of the learned functionality.

The chip layout is shown in Figure 5, highlighting all the components previously described. It is fabricated in a 130nm CMOS process, and occupies an area of $6mm^2$.

V. Conclusion

We summarized the recent developments on post-production calibration methods for analog/RF ICs and provided a taxonomy of the available solutions. Toward addressing most of the shortcomings of the available solutions we introduced a fully integrated mechanism for self-tune and self-calibration of a LNA. The mechanism employs a low-power reconfigurable analog neural network fabricated in 130nm CMOS, which along with tuning knobs and low-cost sensors is capable of optimizing the overall performance of the LNA in the field.

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