Phase Noise Reduction in LC VCO's Using an Array of Cross-Coupled Nanoscale MOSFETs and Intelligent Post-Fabrication Selection

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***Abstract*— Low-frequency noise, thermal noise, and dc characteristics of nanoscale MOS transistors with dimensions close to the process minimum are highly variable. This article demonstrates a phase noise (PN) reduction technique for LC voltage-controlled oscillators (VCOs) that use an intelligent post-fabrication selection of a subset of an array of near minimum-size cross-coupled transistor pairs with reduced low-frequency noise and thermal noise. Using the technique, the PN of a VCO is lowered from the maximum by 3.5 dB at 600-kHz, 1-MHz, and 3-MHz offsets from a 3.8-GHz carrier. The lowest PN of −122, −129, and −139.5 dBc/Hz at 600-kHz, 1-MHz, and 3-MHz offsets, respectively, from a 3.8-GHz carrier has been measured using the PLL method of the Keysight E5052B Signal Source Analyzer. The VCO prototype was fabricated in a 65-nm CMOS process and dissipates 7 mW of dc power. The maximum figure of merit (FoM), including PN, carrier frequency, and power consumption, is 193 dBc/Hz, and the FoM, including the VCO core area, FoM_A, is 209 dBc/Hz.**

***Index Terms*— CMOS, defects, genetic algorithm, LC, low-frequency noise, phase noise (PN), post-fabrication selection, thermal noise, transistor array, variability, voltage-controlled oscillators (VCO).**

I. Introduction

A VOLTAGE-CONTROLLED oscillator (VCO) is a key building block in high-performance wireless and wireline communication systems. The phase noise (PN) of VCOs impacts the system performance in numerous RF and millimeter-wave applications. Adjacent channel rejection, jitter, and error vector magnitude (EVM) of demodulated signals that depend on VCO PN are key factors determining the order of modulation that can be deployed for communication systems to increase the data rate and bandwidth efficiency. For instance, the 3GPP TS 38.101-1 EVM requirements for a wireless receiver employing a 256-QAM modulation scheme for the emerging 5G communication are only 3.5% [1] and become even tighter as the order of modulation increases, which makes the PN and integrated jitter critical in millimeter-wave phased array systems [2], [3]. Similarly, in millimeter-wave radar applications, the low integrated jitter or a low PN of a VCO improves resolution and the probability of detection of radars [4].

To reduce the PN of LC VCOs, numerous circuit topologies have been reported [3]–[19]. The noise of the cross-coupled pair of transistors in CMOS LC VCOs is a major contributor to the overall PN. Upconversion of both the low-frequency noise and thermal noise of cross-coupled transistors is a key mechanism contributing to the PN of LC VCOs [5]–[21].

Scaling of the MOSFETs in advanced CMOS technologies accompanies increased process variation and noise variability. The number of intended dopants and unintended defects in a minimum-sized device is reduced with the technology scaling. One missing dopant or having an additional defect can have a dramatic impact on device characteristics, including threshold voltage, current, and low-frequency noise [22]–[26]. In addition, the thermal noise can also considerably vary due to the variations of the dc properties, such as mobility, effective channel length, threshold voltage, and gate dielectric layer thickness [27]–[29].

This article presents a PN reduction technique in LC VCOs by using an array of individually selectable cross-coupled pairs of transistors [30]. Applying an intelligent post-fabrication selection process [31], [32] in a VCO using the array to select cross-coupled pairs with reduced low-frequency noise and thermal noise, the PN is lowered from the average by 2 dB at 600-kHz and 1-MHz offsets and by 1.5 dB at a 3-MHz offset, respectively, from a 3.8-GHz carrier. It is also lowered by 3.5 dB from the maximum PN at the offset frequencies. The average and maximum PNs should be close to those for a conventional VCO using a cross-coupled pair formed with two transistors but with the same total width as that of the selected cross-coupled pairs in the array. The lowest PN of −122, −129, and −139.5 dBc/Hz at 600-kHz, 1-MHz, and 3-MHz offsets, respectively, from a 3.8-GHz carrier has been measured using the phase-locked loop (PLL) method without correlation and with an averaging of 50 in the Keysight E5052B Signal Source Analyzer.

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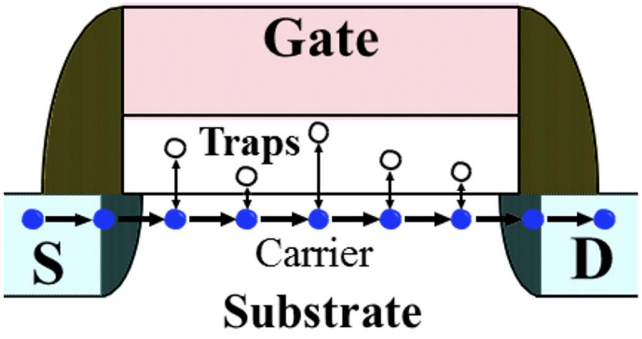

Fig. 1. Trapping–detrapping process in a gate dielectric layer of MOSFETs [34].

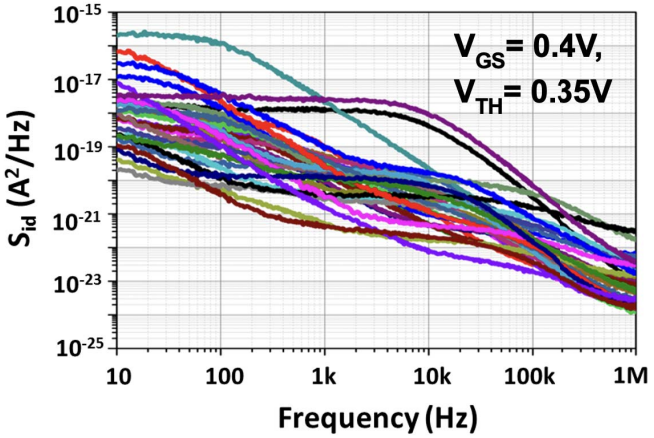

Fig. 2. Measured low-frequency noise variability of 32 nMOS transistors with dimensions near the minimum in a 65-nm CMOS process ($W = 150$ nm, $L = 60$ nm, and Area $= 9000$ nm^2).

This article is an extension of work in [30] where the concept and some of the preliminary measurement results were introduced. This article by elimination: 1) demonstrates that the variation of observed PN is due to the low-frequency noise variation; 2) reports that the variation of thermal noise in near minimum-sized transistors can also be exploited to lower the PN; and 3) demonstrates the use of a more efficient algorithm for searching combinations with lower noise in high-dimensional unstructured spaces. Unlike the works in [31] and [32] that utilized the variation of static device parameters and post-fabrication selection to lower offsets, this work utilizes the variability of thermal noise and reduced low-frequency noise at the lower end of low-frequency noise distribution in near minimum-sized transistors with intelligent post-fabrication selection to lower the PN of 4-GHz VCOs.

This article is organized as follows. Sections II and III describe the variability of low-frequency and thermal noise in MOS transistors, respectively, and how these variabilities can be advantageously used to lower the PN of LC VCOs. Section IV presents the proposed VCO using an array of cross-coupled transistor pairs with size near the process minimum. Section V describes the intelligent-search genetic algorithm used for the post-fabrication selection. Finally, Section VI reports the measurement results before concluding.

II. Low-Frequency Noise Variability

The McWhorter model [33] attributes the trapping and detrapping processes of the channel electrons or holes in a gate oxide or dielectric region as the generation mechanism for low-frequency noise of MOSFETs, as shown in Fig. 1. The properties of traps determine the power spectral density (PSD) and corner frequency. The PSD of each individual trap, also called a Lorenztian that originates random telegraph noise (RTN), can be added to generate the $1/f$-noise spectrum [33], [34]. Since the number of traps in a large area device is large, the low-frequency noise variation from device to device is reduced because the sum of all the PSDs averages the variations due to individual traps.

However, in nanoscale transistors, the number of traps in the Si-gate dielectric layer decreases to a few or less than one per transistor. Such transistors do not exhibit the $1/f$-noise spectrum that requires averaging the effects of a large number of traps [35]–[39]. The defect density related to low-frequency noise in nanoscale CMOS is $\sim 1 \times 10^9$ cm^{-2} (kTN_{ot}/α_t of [23, eq. (1)]), which translates to on average, one trap in $\sim 300 \times 300$ nm^2 or $\sim 90\,000$ nm^2, which is larger than the area of minimum-sized transistors in nanoscale CMOS. In such MOSFETs, the number of traps is not a fixed process constant but rather a random variable whose uncertainty increases with a shrinking device size. This leads to a large variation of low-frequency noise for otherwise similar devices sized near the minimum. In addition, even if the number of traps is the same, the locations of traps in the dielectric layer can be different, which also results in dissimilar Lorenztians and, therefore, an increase in the low-frequency noise variation [35]–[39].

Fig. 2 shows the measured low-frequency noise of 32 nMOS transistors with a width and a length of 150 and 60 nm, respectively, or for a gate area of ~ 9000 nm^2. The transistors are biased at $V_{GS} = 0.4$ V, $V_{DS} = 0.6$ V, and $V_{TH} = \sim 0.35$ V. From the plot, it can be observed that the drain current noise spectral density varies by four orders of magnitude at 10 kHz and three orders of magnitude at 1 MHz. This large variation is attributed to the fact that the number of traps in the transistors is not the same, as well as to the fact that dc current varies due to the variation of transistor parameters, such as effective channel length, mobility, gate dielectric thickness, and threshold voltage [27]–[29]. The average low-frequency noise in the PDK is dominated by a few devices with the highest noise. In addition, some of the transistors can have noise significantly lower than the average low-frequency noise.

Fig. 3 shows the maximum and minimum current noise spectral densities of a set of ten transistors randomly selected from the array of 32 transistors. The minimum current noise spectral density is an order of magnitude lower than the normalized sum predicted by the PDK. This implies that, if only the transistors with low noise can be used by post-fabrication selection, then it should be possible to significantly reduce the low-frequency noise impact. Using minimum-sized transistors to reduce the low-frequency noise is opposite

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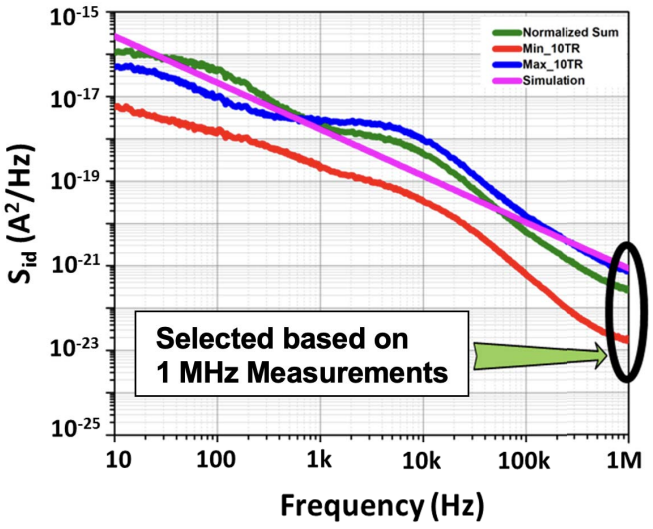

Fig. 3. Current noise PSD of combinations formed by randomly selecting ten transistors out of 32.

to the conventional approach of reducing the impact of low-frequency noise by using larger transistors, which relies on averaging the value determined by the PDK model. Because of this, the approach using post-fabrication selection can result in circuits with significantly reduced impact of low-frequency noise.

III. Thermal Noise Variability

The channel thermal noise of an MOS transistor operating in a saturation region can be modeled by a current source [40]. The current noise spectral density is

$$\bar{i_{n,d}^2} = 4kT\gamma g_{d0} \tag{1}$$

where g_{d0} is the zero-bias drain conductance of the device and γ is a bias-dependent coefficient of thermal noise, which can be much greater than one for short-channel MOS transistors [41]. The zero-bias drain conductance, g_{d0}, and the transconductance, g_m, are related by the factor α [41], as shown in the following equations:

$$\alpha \triangleq \frac{g_m}{g_{d0}}. \tag{2}$$

For short-channel MOS transistors, α can be much less than one. It is well known that g_m in terms of bias voltages (V_{GS}, V_{DS}), threshold voltage (V_{TH}), width (W), length (L), mobility (μ_n), and gate capacitance (C_{ox}) of a long-channel MOS transistor is

$$g_m = \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{TH})(1 + \lambda_n V_{DS}). \tag{3}$$

After substituting the equations for α and g_m in (1), the current noise spectral density is

$$\bar{i_{n,d}^2} = \frac{4kT\gamma}{\alpha} \cdot \left[\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{TH})(1 + \lambda_n V_{DS})\right]. \tag{4}$$

It can be observed from (4) that the thermal current noise spectral density of an MOS transistor depends on its mobility, physical dimensions, bias voltages, threshold voltage, oxide capacitance, and coefficients α, γ, and λ. As shown in Fig. 4(b), the dc bias voltages (V_{GS}, V_{DS}) are kept constants for all the selected cross-coupled pairs in the array used to implement the proposed VCO. However, the other parameters in (4), such as mobility, effective channel length, threshold voltage, and gate dielectric layer thickness, can significantly vary [27]–[29], which leads to the thermal noise variation. This implies that, if only the transistors with lower thermal noise can be used by post-fabrication selection, then it should also be possible to reduce the thermal noise impact on the overall PN.

IV. VCO Using an Array of Near Minimum-Sized Transistors

To demonstrate the technique of reducing the impact of low-frequency noise and thermal noise in an LC VCO by using an array of transistors sized near the minimum and post-fabrication selection, a VCO operating around 4 GHz [30] using an array of cross-coupled pairs of near minimum-size transistors is implemented. To start, a conventional VCO using a cross-coupled nMOS pair of 8 μm width and 60 nm length with an nMOS tail current source, as shown in Fig. 4(a), is first designed. By using a long and wide nMOS tail current transistor of 150 μm width and 500 nm length, the noise of the cross-coupled devices is made the dominant source. A high-Q 8-pF bypass capacitor at the drain node of the current source effectively prevents the injection of the thermal noise of current source transistor to the oscillator core [42].

The top plate of varactors is connected to V_{DD} through the tank inductor. The 2.5-nH tank inductor is formed with a five-turn circular symmetric center-tapped structure. It has a simulated Q-factor of 12 at 4 GHz. The varactors are of an accumulation mode type implemented as an nMOS structure in an n-well [43]. Fig. 4(b) shows the proposed VCO that uses an addressable array of 16 $\times$ 4 (64) nMOS cross-coupled transistor pairs for post-fabrication selection of pairs with reduced low-frequency and thermal noise. Each transistor forming the cross-coupled pair in Fig. 4(a) is divided into 32 transistors of a width and a length of 250 and 60 nm, respectively, or an area of 15 000 nm^2. To provide redundancy, 32 additional pairs are added. Each unit also includes 2.5-μm wide switches at the drains of the cross-coupling transistors for selection.

The selection switches for a pair can be placed at the gate, drain, or source of the transistors, as shown in Fig. 5. The PN with the switch at the gate of the transistor is worse than that for the VCO with the switch at the drain of the transistor for the same switch size. This is due to the switch resistance being in series with the gate impedance of the cross-coupled transistors. The thermal noise associated with the ON-resistance, R_{on} of switch has more impact for the gate-switched core compared to that of the drain-switched core. When referred to the output, the noise of the switch at the gate is amplified by the transistor gain, resulting in a higher noise contribution compared to that of the drain-switched core. The ON-resistance also lowers the output swing. The switch

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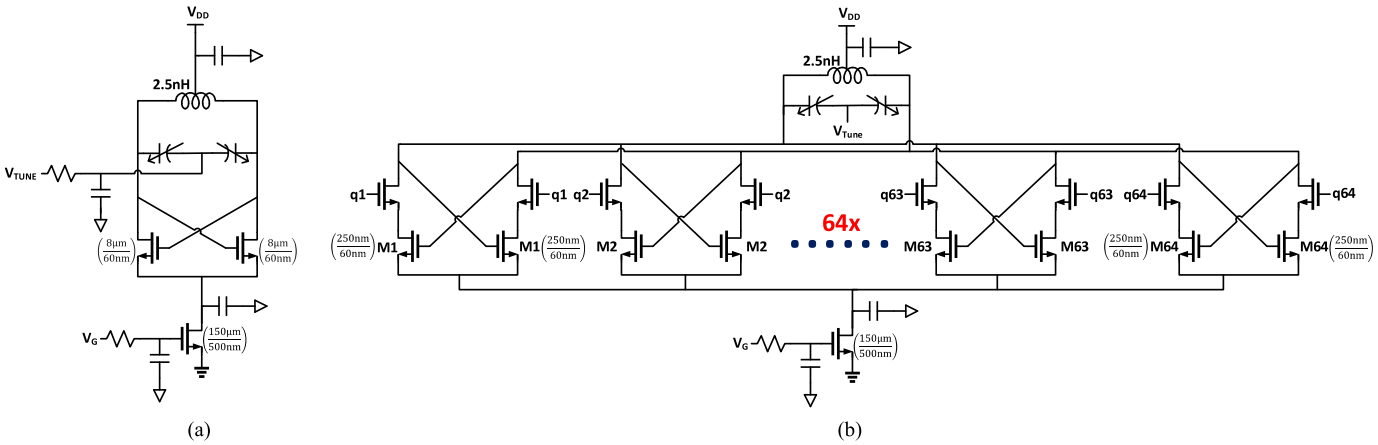

Fig. 4. (a) Conventional nMOS VCO. (b) Proposed VCO using an array of cross-coupled near minimum-sized nMOS transistor pairs.

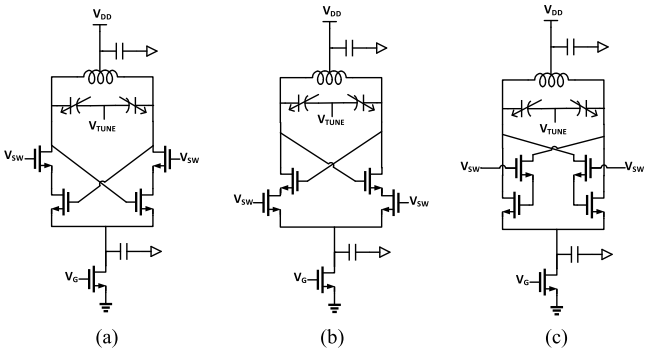

Fig. 5. (a) Drain-switched core. (b) Source-switched core. (c) Gate-switched core.

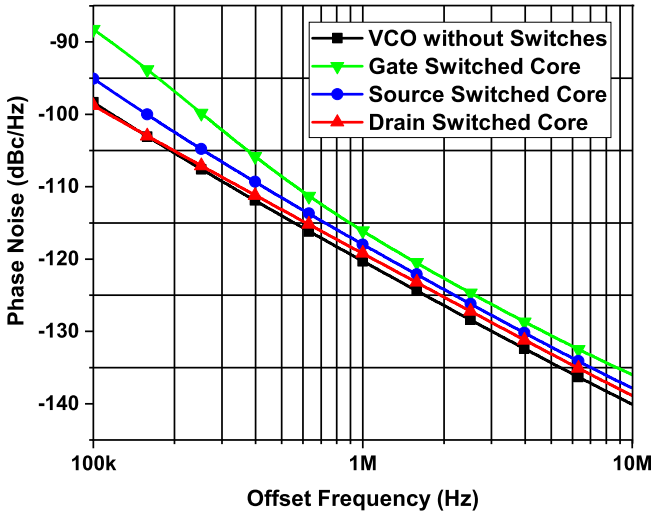

Fig. 6. Simulated PN of VCO with and without switches for post-fabrication selection.

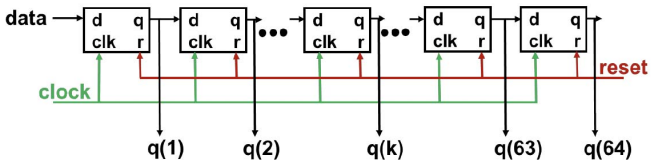

Fig. 7. Block diagram of the 64-bit SIPO chain of D flip-flops.

at the gate can be sized larger to reduce the gate resistance, but this, however, increases the parasitic capacitances of the switch and the cell area.

The source-switched core topology has a lower output swing than that of the drain-switched core due to the degeneration effect caused by the switch resistance at the source of core transistors. This, in turn, makes the PN of the source-switched core higher compared to that of the drain-switched core. Fig. 6 shows the simulated PN of a VCO using the array with different placements of switches at the tuning voltage of 0 V and with 32 cross-coupled transistor pairs switched ON. A switch with 2.5 μm width and 60 nm length is used. The PN of VCO using the array with the drain switched core at a 1-MHz offset is -119 dBc/Hz from a 3.83-GHz carrier, whereas the PN of the gate switched core is -116 dBc/Hz at a 1-MHz offset, which is 3 dB higher than that of the drain switched core. The PN of the source switched core is -118 dBc/Hz at a 1-MHz offset, which is 1 dB higher than that of the drain switched core.

The switches for the 64 pairs of cross-coupled transistors are controlled by a 64-bit serial-in–parallel-out (SIPO) D flip-flop chain. The D flip-flop is falling edge-triggered. A block diagram of the 64-bit SIPO is shown in Fig. 7. The switch size, as mentioned earlier, is chosen to ensure the additional parasitics of the switches do not significantly degrade both the PN performance and tuning range of the VCO using the array compared to that of the conventional VCO. Fig. 6 also shows the simulated PN of the conventional VCO at a tuning voltage of 0 V. Compared to the VCO without switches, there is $\sim$1-dB PN degradation for the VCO using the array with drain-side switching. The PN of the conventional VCO is -120 dBc/Hz at a 1-MHz offset from a 3.98-GHz carrier.

Fig. 8 shows the tuning range comparison between the conventional VCO without switches and VCO using the array with drain side switching and 32 cross-coupled pairs switched ON. The conventional VCO without switches oscillates from

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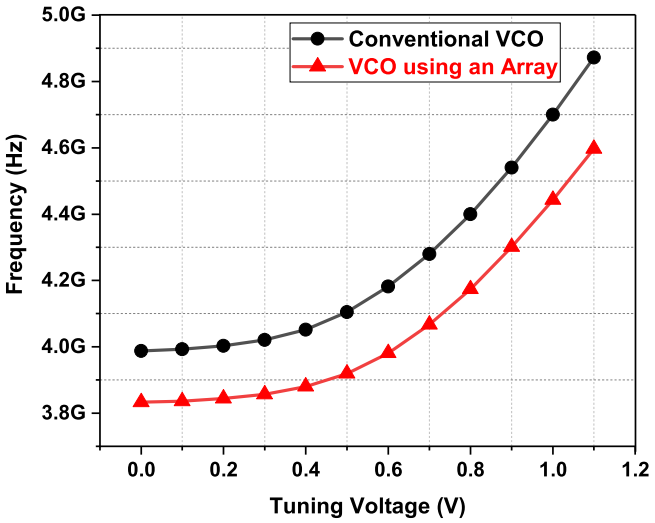

Fig. 8. Tuning ranges of the Conventional VCO without switches and VCO using an array with drain side switching.

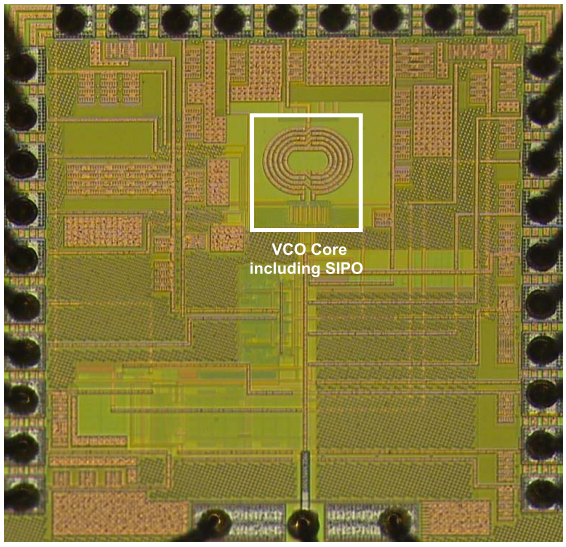

Fig. 10. Die micrograph.

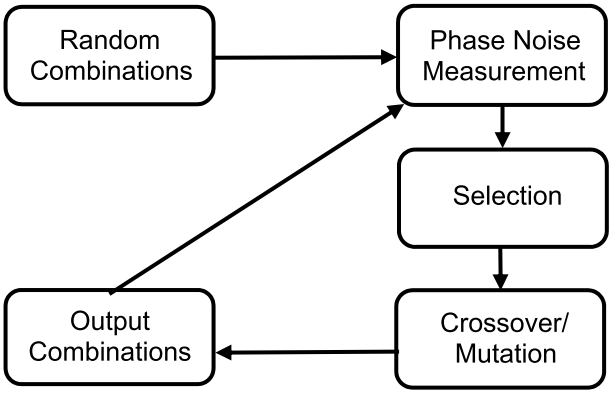

Fig. 9. Flowchart of the genetic algorithm.

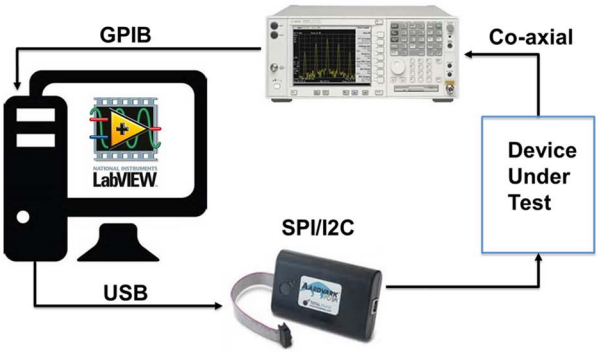

Fig. 11. Measurement setup for PN.

3.98 to 4.87 GHz, which corresponds to a simulated tuning range of 20%. The VCO using the array with drain side switching achieves a simulated tuning range of 18% from 3.83 to 4.59 GHz, which is only 2% smaller compared to the tuning range of conventional VCO.

V. Intelligent Search via Genetic Algorithm

Searching among the vast space of 2^{64} possible combinations of switched-ON cross-coupled transistor pairs to identify the ones having a given PN target requires an intelligent algorithm. A Hamming distance-driven search [30] explores a predetermined number of options in the Hamming distance vicinity of an initial seed and may converge to a local minimum. Instead, a classic genetic algorithm, which introduces more entropy in the search and is particularly efficient in exploring high-dimensional unstructured spaces, is employed. In addition, the genetic algorithm makes no assumptions about the search space and is driven by randomness, which makes it superior in searching for the combinations having low PN in a large space. A flowchart of the genetic algorithm is shown in Fig. 9. It defines the PN at a particular offset frequency as a "fitness function" to be optimized.

Each cross-coupled transistor pair is represented by a bit, with a value of "1" indicating that the pair is switched ON. The algorithm starts by generating a random population of chromosomes (i.e., binary strings with a varying length) with a user-defined range of the number of "1"s for which the fitness function is measured. The top 50% of the initial population with the lowest PN is retained, and the rest of the population is discarded. The binary strings in the top 50% of the population are named "parent strings."

The population is then replenished with new chromosomes by mutating the pairs of parent strings at a randomly chosen bit-location, called a "crossover point". All the bits to the right of the crossover point are swapped between the pairs of parent strings to generate new offspring strings. The rationale of this operation is that, after multiple generations, the mutation will allow a sufficiently diverse space to be explored, while the crossover will discard the bits having high PN in the parent strings, thereby generating new offspring strings with lower PN. The algorithm continues until a fitness limit specified by a user is achieved or until a sufficient number of combinations with adequately low PN are found.

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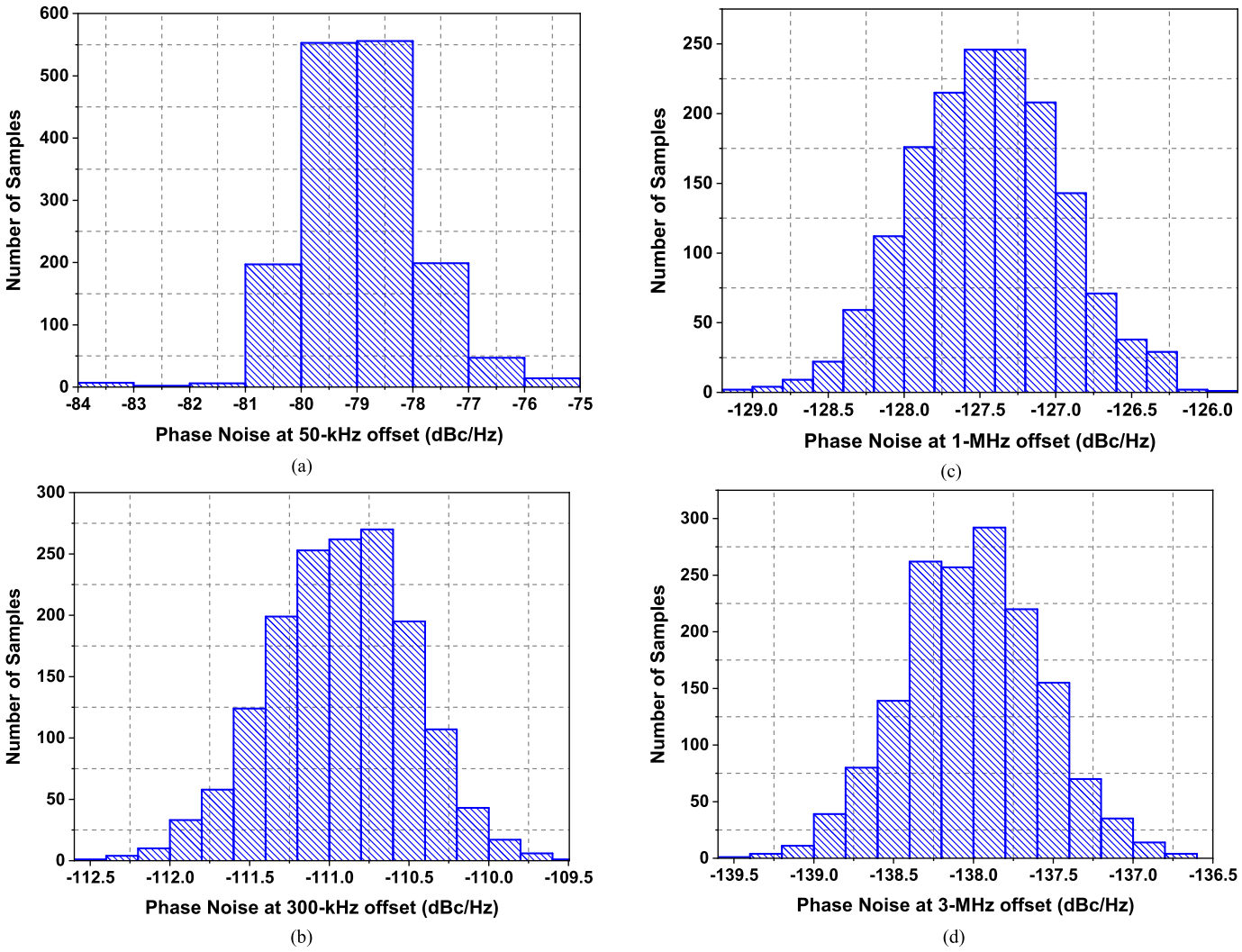

Fig. 12. Histograms of PN at (a) 50-kHz offset, (b) 300-kHz offset, (c) 1-MHz offset, and (d) 3-MHz offset from a 3.8-GHz carrier when 32 cross-coupled transistor pairs are switched ON.

VI. Measurement Results

A prototype of the proposed VCO was fabricated in a 65-nm CMOS process with ten copper layers and one aluminum bond pad layer, and wire-bonded onto a printed circuit board (PCB) for measurements. The die micrograph is shown in Fig. 10. The core area of the VCO, including SIPO, is 0.025 mm^2. A setup for measuring the PN with different combinations of cross-coupled pair units is shown in Fig. 11. 32 of the 64 cross-coupling transistor pairs are switched ON in the VCO by sending a random set of 32 "1" bits using LabVIEW to the DUT using an SPI/I2C interface. PN is measured using the PLL method of the Keysight E5052B Signal Source Analyzer with an average of 50 and is collected using LabVIEW. Fig. 12 shows the histograms of measured PN variations of ∼1500 combinations at 50-kHz, 300-kHz, 1-MHz, and 3-MHz offsets from a 3.8-GHz carrier, respectively, when 32 cross-coupled transistor pairs out of the 64 pairs are switched ON. Fig. 13 shows the PN plots of these 1500 combinations.

Two main observations can be made from these figures: 1) from 10-kHz offset to 60-kHz offset, PN variation is around 9 dB, which mainly is due to the low-frequency noise variation of the core devices being the dominant determining factor and 2) PN variation is ∼3.5 dB at higher offsets of 1 and 3 MHz, respectively. The PN variation decreases with an increasing offset because the contributions of thermal noise increase at higher frequency offsets.

It can also be noted from Fig. 13 that the lowest PN is 9 dB lower than the maximum PN at a 50-kHz offset, whereas it is ∼3–3.5 dB lower than the maximum PN at 1- and 3-MHz offsets. Fig. 14 shows the histograms of PN variations of ∼1500 random combinations at 50-kHz and 1-MHz offsets from a 3.78-GHz carrier when 48 cross-coupling transistor pairs out of the 64 pairs are switched ON. The PN variations are ∼7 dB at a 50-kHz offset and ∼2.5 dB at a 1-MHz offset. These variations are 2 and 1 dB lower than that when 32 pairs are selected out of 64, respectively.

The reduction of PN variation with an increasing number of switched-ON cross-coupling pairs can be attributed mainly to the law of large numbers. In addition to the variations in low-frequency noise and the thermal noise, variations in the carrier

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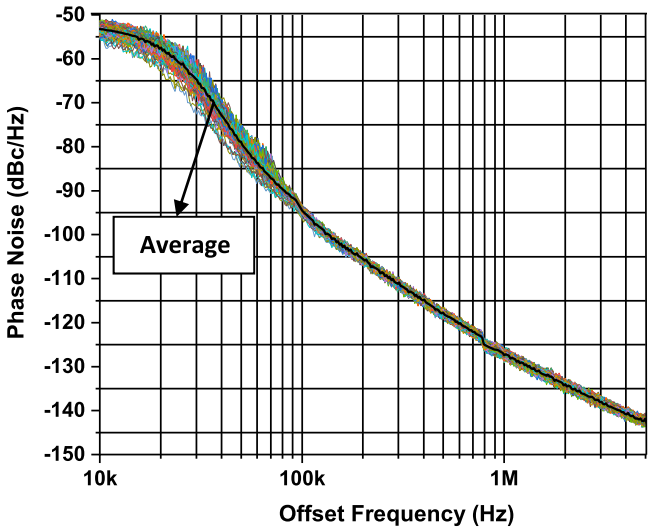


Fig. 13. Measured PN plots when 32 cross-coupled transistor pairs are switched ON. Average PN is also shown in the figure.

power of cross-coupling transistor pairs can also contribute to the PN variation. The variation of the output power for the combinations with an equal number of cross-coupled pairs switched ON should be mainly due to the variations in the VCO bias current and parallel resistance R_p of the tank due to the variations of the output resistance of the cross-coupling transistor pairs.

The output power (P_o) in an LC VCO is directly proportional to the square of the product of the current flowing through the cross-coupled pairs ($I_{\rm cp}$) and the total parallel resistance (R_p) in the tank [40], as given in the following equation:

$$P_o \propto \left(I_{\rm cp} R_p\right)^2. \tag{5}$$

Since $I_{\rm cp}$ is set by the current source, the power variation should be mostly due to the variation of R_p. Neglecting the losses due to the gate resistance, substrate resistance, and varactor, R_p, as shown in (6), can be given by the parallel combination of the equivalent resistance (R_{pL}) of inductor and output resistance ($R_{\rm ds}$) of the transistors in the cross-coupled pairs [44]

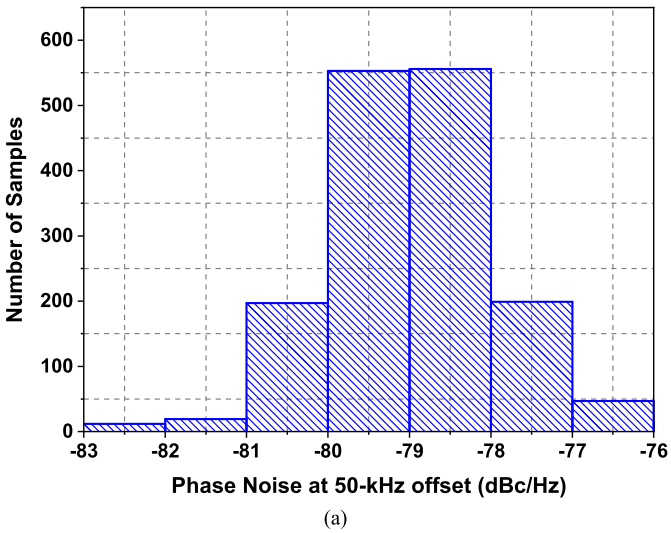
$$R_p = R_{pL} \| R_{\rm ds}. \tag{6}$$

The total $R_{\rm ds}$ in the VCO array is given by the following equation:

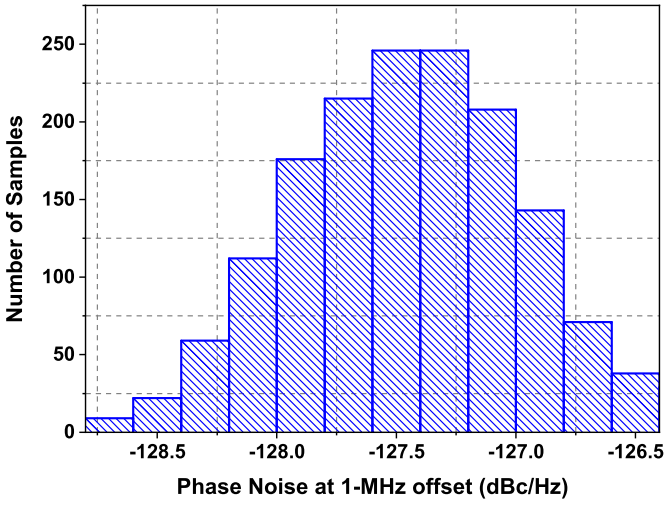
$$R_{\rm ds} = R_{{\rm ds},1} \| R_{{\rm ds},2} \| R_{{\rm ds},3}, \ldots, R_{{\rm ds},n} \tag{7}$$

where $R_{{\rm ds},1}$–$R_{{\rm ds},n}$ are the output resistances of a single transistor from each selected cross-coupled transistor pair, and n is the total number of pairs switched ON out of 64.

Fig. 15(a) and (b) shows the correlation between the carrier power and PN at 50-kHz and 1-MHz offsets, respectively, when 32 cross-coupled transistor pairs are switched ON. Randomly chosen subsets of combinations from PN bins in Fig. 13 are selected for carrier power measurements. The variation in carrier power is only ~1 dB for 32 selected pairs. A maximum PN variation of ~6 dB is observed at a carrier power of −11.6 dBm at a 50-kHz offset, and the correlation



(a)



(b)

Fig. 14. Histograms of PN at (a) 50-kHz offset and (b) 1-MHz offset from a 3.78-GHz carrier when 48 cross-coupled pairs are switched ON.

coefficient using the linear fit shown in Fig. 15(a) is only 3%, whereas, at a 1-MHz offset, a maximum PN variation of ~3 dB is observed at multiple carrier power levels (−11.6, −11.7, and −12 dBm), and the correlation coefficient using the linear fit shown in Fig. 15(b) is only 9%. These results indicate that the variation of PN is not due to the carrier power variation.

Fig. 16 shows the PN at 1 MHz versus that at 50 kHz for the samples used for the histograms in Fig. 13. The PN at a 50-kHz offset limited by the low-frequency noise is not correlated with the PN at a 1-MHz offset where the thermal noise contribution dominates. The correlation coefficient using the linear fit shown in the figure is only 7%. The correlation of low-frequency noise to thermal noise due to correlated increased mobility due to lower trap density [45] is not observed. The genetic algorithm for post-fabrication selection is coded in Python and integrated with LabVIEW. Offset frequencies of 50 kHz, 1 MHz, and 3 MHz were used in the genetic algorithm to lower the PN. Around 100 combinations were generated by the algorithm in each generation. The user-defined range for the number of selected cross-coupling pairs is between 20 and 60.

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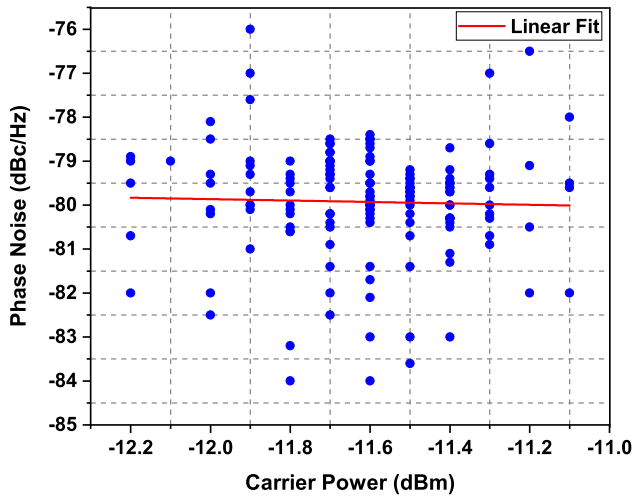
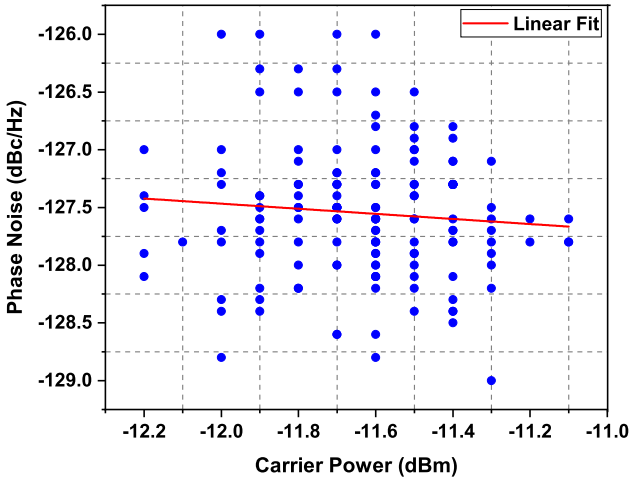


(a)



(b)

Fig. 15. PN versus Carrier Power at (a) 50-kHz offset and (b) 1-MHz offset from the 3.8-GHz carrier when 32 cross-coupled pairs are switched ON.

Fig. 17 shows the measured lowest PN at 50-kHz, 1-MHz, and 3-MHz offsets, respectively, at varying generations. The genetic algorithm converges to the combinations having the lowest PN of −84 dBc/Hz at a 50-kHz offset, −129 dBc/Hz at a 1-MHz offset, and −139.5 dBc/Hz at a 3-MHz offset, respectively, from a 3.8-GHz carrier. Fig. 18 shows the PN plot of the best combination having the lowest PN of −129 dBc/Hz at a 1-MHz offset from a 3.8-GHz carrier when 32 cross-coupling pairs are selected. The slope of −2 is also shown in the figure, which is between 900-kHz and 9-MHz offsets.

The lowest PN when 32 pairs are switched ON is 0.5 dB lower at a 1-MHz offset than that for the best combination when 48 pairs are selected, whereas the PN when all the 64 pairs are switched ON is −126.5 dBc/Hz at a 1-MHz offset, which is 2.5 dB higher than that for the best combination having 32 selected pairs. Raising the number of selected cells increases the overall transistor width while keeping the VCO dc current constant due to the tail current source. This increases the transconductance while keeping R_{ds}; thus, R_P is approximately constant, thereby increasing the VCO loop gain $(g_m R_p)^2$. This indicates that the PN of VCO using the array is not reduced due to an increase in the VCO loop gain.

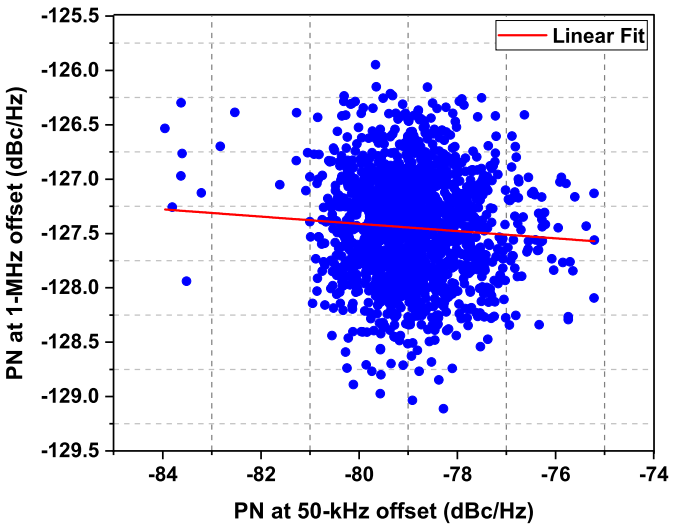


Fig. 16. PN at 1-MHz offset versus that at a 50-kHz offset when 32 cross-coupled transistor pairs are switched ON.

Variations of the VCO gain (K_{vco}) among different combinations of selected cross-coupled pairs can also contribute to the PN variation since a higher VCO gain leads to higher PN due to increased AM–PM conversion and vice versa [46], [47]. Fig. 19 shows the PN at a 1-MHz offset versus measured VCO gain for the samples used for the histograms in Fig. 12. 32 cross-coupled transistor pairs were switched ON. The VCO gain shown in the figure is measured for a tuning voltage at 0.05 V near which the measured PN is minimum. As observed in Fig. 19, the maximum PN variation of ∼3 dB is observed at the VCO gains of 30 and 40 MHz/V. The correlation coefficient using a linear fit shown in Fig. 20 is only 10%. This shows that the PN variations of the VCO using the array are not due to variations of the VCO gain.

This process of elimination and the fact that PN can vary by many dBs at a given VCO output power and gain suggest that the likely cause for the PN variation is the variations of the low-frequency noise and the thermal noise. The increase in PN by 2.5 dB when all the 64 pairs are switched ON compared to the case when 32 pairs are selected shows that there exists some pairs of transistors having high thermal noise and low-frequency noise, and these pairs should be discarded to reduce the PN. The VCO was characterized using the PLL method in E5052B because multiple works reporting low PN VCO have used the PLL method of E5052B for their measurements [16], [20].

The VCO in this work was also characterized using the PN utility in Keysight E4440A PSA. The lowest PN measured using the E4440A PSA is 11 dB higher than that in E5052B. Improvements are expected from using the PLL method in E5052B because it locks the free-running VCO to measure its PN. The 11-dB difference seems large. Measurements were checked and repeated multiple times to ensure the proper operation of the instruments. Because of this, the figure of merit (FoM) in (8) normalizing the oscillation frequency (f_o), power dissipation (P_{dc}), and PN (L_{offset}) at a particular offset frequency (f_{offset}) have been estimated from the measurements

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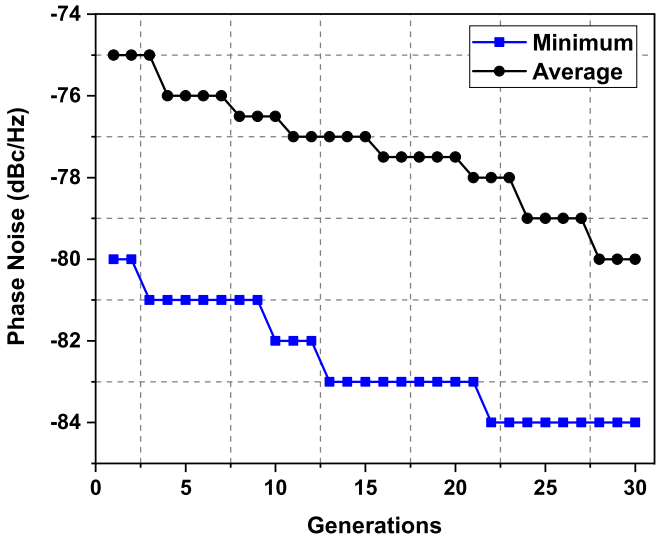
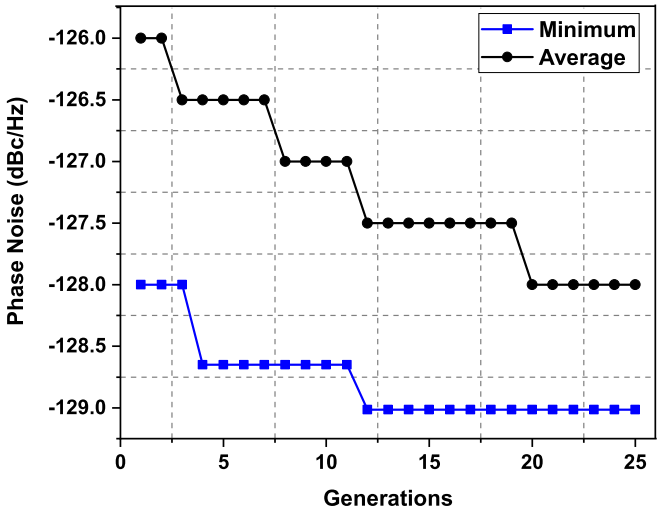


(a)



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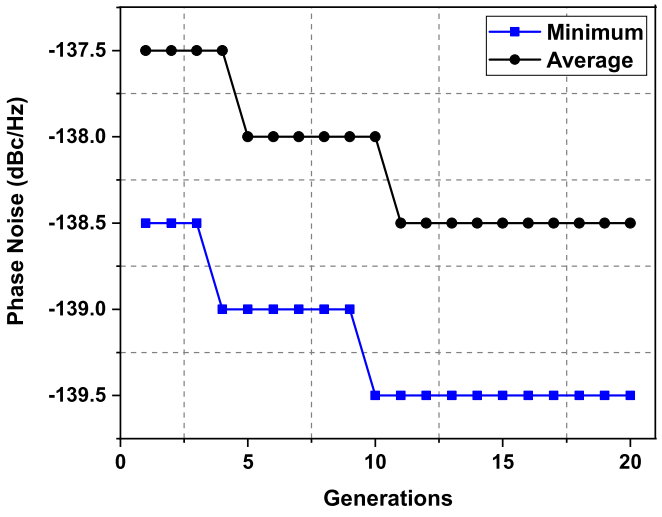

(c)

Fig. 17. PN reduction using the Genetic algorithm at (a) 50-kHz offset, (b) 1-MHz offset, and (c) 3-MHz offsets from a 3.8-GHz carrier.

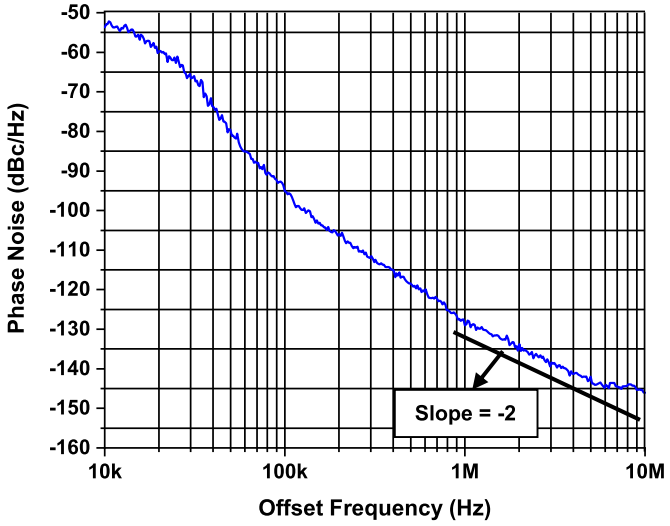

Fig. 18. PN of the best combination having the lowest PN at a 1-MHz offset from a 3.8-GHz carrier.

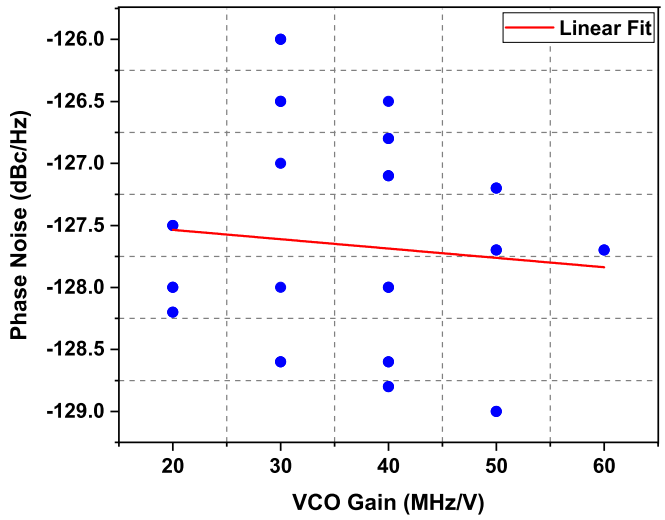

Fig. 19. PN at 1-MHz offset versus VCO gain when 32 cross-coupled pairs are switched ON.

from both E4440A PSA and E5052B

$$\text{FoM} = 20\log\left(\frac{f_0}{f_{\text{offset}}}\right) - L_{\text{offset}} - 10\log\left(\frac{P_{\text{dc}}}{1\ \text{mW}}\right). \quad (8)$$

Fig. 20(a) and (b) shows the PN and FoM at a 1-MHz offset across the measured tuning range of 3.8–4.1 GHz for the best combination, respectively. There is ∼3-dB variation of PN at a 1-MHz offset across the tuning range. The peak FoM of 192 dBc/Hz at a 1-MHz offset is achieved at the minimum frequency of 3.8 GHz where the tuning voltage is 0 V. The FoM measured in the PSA is 11 dB lower than that in E5052B. There is ∼2-dB variation of FoM across the tuning range. This is due to the PN degradation at higher tuning voltages, which, in turn, is caused by the higher AM–PM conversion due to higher VCO gains [46], [47]. This problem can be resolved by linearizing the VCO tuning curve with a programmable capacitor bank and, thereby, maintaining a lower K_{vco} over the entire tuning range [48]. Nevertheless, the VCO still achieves

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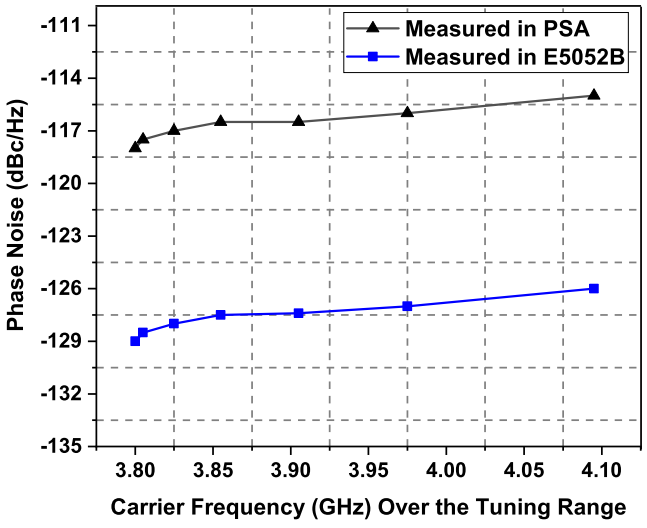
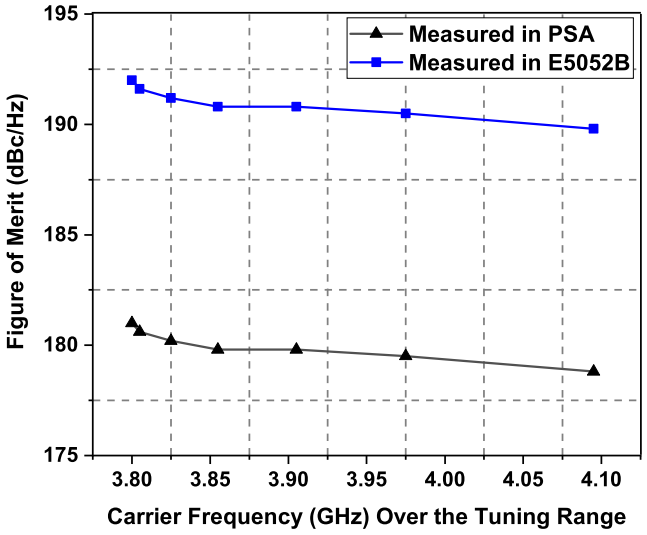


(a)



(b)

Fig. 20. (a) PN at 1-MHz offset and (b) FoM at 1-MHz offset for the best combination across the tuning range.

an FoM of greater than 189.5 dBc/Hz (measured in E5052B) over the tuning range. Fig. 21 shows the output power across the tuning range. Compared to the simulated output power, there is only 0.5-dB degradation in the measured output power across the tuning range for the best combination.

Table I summarizes the improvements of PN from the average and maximum PNs at various offsets from the 3.8-GHz carrier. The PN at a 50-kHz offset is lowered by 5–6 dB from the average PN in the measurements done in both PSA and E5052B, and by 9 dB from the maximum in E5052B and by 12 dB in PSA, whereas at 600-kHz, 1-MHz, and 3-MHz offsets, it is lowered by 1.5–2 dB from the average and ∼3.5 dB from the maximum. Both the measurements using the PSA and E5052B show that PN can be lowered by applying an intelligent post-fabrication selection process to a VCO employing an array of individually selectable cross-coupled pairs of transistors with dimensions near the minimum for a given process.

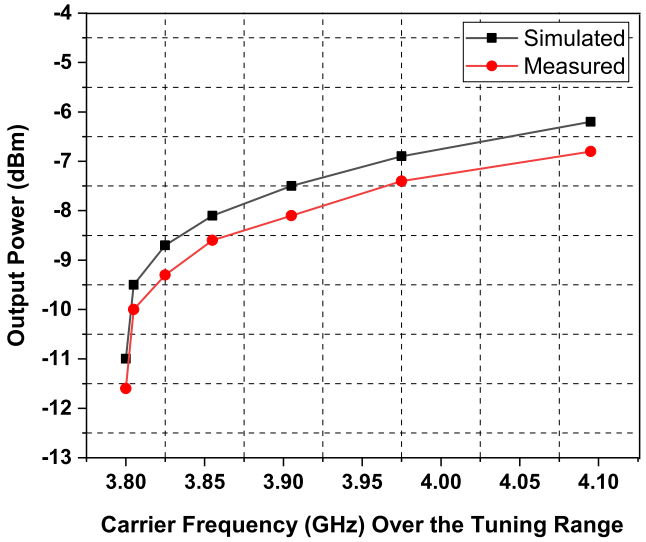


Fig. 21. Output Power across the tuning range for the best combination.

TABLE I
PN IMPROVEMENT FROM AVERAGE AND MAXIMUM AT VARIOUS OFFSET FREQUENCIES

Offset	Improvement from Average (in E5052B)	Improvement from Max (in E5052B)	Improvement from Average (in PSA)	Improvement from Max (in PSA)
50 kHz	5 dB	9 dB	6 dB	12 dB
600 kHz	2 dB	3.5 dB	2 dB	3.5 dB
1 MHz	2 dB	3.5 dB	2 dB	3.5 dB
3 MHz	1.5 dB	3 dB	1.5 dB	3.5 dB

Table II summarizes the performance and benchmarks the proposed VCO using an array of cross-coupled pairs in this article with that of the other low PN CMOS LC VCOs in the literature. The main aim of this article is to verify the proposed technique. The peak FoM of the VCO array is 193 dBc/Hz at a 3-MHz offset from a 3.8-GHz carrier. Another FoM, FoM_A that also takes the core area of VCO into account, is calculated for all the works and included in the table. The VCO in this article exhibits an excellent FoM_A of 209 dBc/Hz when the PN is measured using the PLL method in E5052B. Even from the PSA measurements, FoM_A of 198 dBc/Hz is on par with the recently published low PN CMOS LC VCOs.

An important point to note is that the proposed technique for reducing PN using post-fabrication selection of transistor pairs sized near the minimum should be orthogonal to the other PN reduction techniques in the literature since the proposed method reduces the device noise itself. For instance, it can be used along with the harmonic shaping technique in a Class-F VCO and achieve an ultralow PN. A Class-F VCO creates a pseudosquare oscillation voltage in order to reduce its impulse sensitivity function, thus lowering the conversion sensitivity of various noise sources to the PN [17]. This along with the reduced device noise resulting from the technique proposed in this article should lead to lower PN. Finally, it should be possible to integrate an on-chip PN measurement circuit in order to make this technique more practical [49]–[54].

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TABLE II
PERFORMANCE BENCHMARK WITH THE STATE-OF-THE-ART CMOS LC VCOS

	VCO Topology	Frequency (GHz)	PN at 1-MHz offset (dBc/Hz)	Power Dissipation (mW)	Tuning Range (%)	PN at 1-MHz offset (dBc/Hz) Normalized to 5 GHz	Peak FoM (dBc/Hz)	Core area (mm^2)	[1] Peak FoM_A (dBc/Hz)	CMOS Technology
This Work (PLL Method in E5052B)	Class-B NMOS VCO using Post-Fabrication Selection	3.8	-129	7	7.8	-126.6	193	0.025	209	65nm
This Work (E4440A PSA)		3.8	-118	7	7.8	-115.6	182	0.025	198	
[5] ISSCC'21	Wideband Harmonic Shaping	5	-130*	6.1	23.9	-130	196.2	0.24	202.4	65nm
[6] ISSCC'21	Multi-Core Harmonic Shaping	3.09	-138.9	20.9	26.6	-134.7	195.1	0.36	199.5	40nm
[7] TMTT'20	VCO using an Inversion mode Varactor	4.14	-109	0.82	40.3	-107.4	185	0.436	188.6	40nm
[8] JSSC'18	Inverse Class-F	4	-124.3	1.2	25.5	-122.3	195.5	0.14	204	65nm
[9] VLSI'17	Pulse-Tail Feedback	4.55	-123.4	1.35	5.5	-122.6	195.3	N/A	N/A	180nm
[10] JSSC'16	Class-$F_{2,3}$	5.4	-126.7	12	25	-127.3	190.5	0.13	199.3	40nm
[11] ISSCC'16	$2f_o$ Implicit Resonance	4.83	-119	0.5	13.8	-118.7	195.7	0.18	203.1	28nm
[12] JSSC'15	Class-F_2	4.35	-135*	41.6	19	-133.8	191.6	0.2	198.6	65nm
[13] ISSCC'15	ISF Manipulation	2.4	-128.4	4.2	1.7	-122	189.8	0.09	200.2	130nm
[14] RFIC'15	Harmonic VCO	5.8	-117*	8	70	-118.3	183.3	0.27	189	28nm
[15] RFIC'15	Class-B Mode Switching	6.48	-114*	2.2	74.6	-116.3	186.8	0.126	195.8	65nm
[16] ISSCC'14	Class-B Mode Switching	3.72	-129.3	20	88.7	-126.7	187.7	0.432	191.3	40nm
[17] JSSC'13	Class-F	3.7	-131	15	25	-128.4	190.6	0.12	199.8	65nm
[18] JSSC'13	Class-C	3.42	-127*	6.6	28	-123.7	189.5	0.08	200.5	90nm
[19] TMTT'13	VCO using a Segmented Transconductor	2.1	-124	8	47.6	-116.5	181.4	0.121	190.6	65nm
[20] JSSC'12	Class-B Mode Switching	3.69	-128.3	10.4	76.5	-125.6	189.5	0.294	194.8	65nm
[21] RFIC'11	VCO using a 5-Port Inductor	4.4	-120	7.1	199	-118.9	184.4	0.36	188.8	180nm

*Estimated from the phase noise plot [1] $FOM_A = 20\log\left(\frac{f_0}{f_{offset}}\right) - L_{offset} - 10\log\left(\frac{P_{DC}}{1mW}\right) - 10\log(\frac{Area}{1mm^2})$

VII. CONCLUSION

A technique for reducing the PN of LC VCOs by employing an array of individually selectable cross-coupled pairs formed using transistors with dimensions near the minimum and by employing an intelligent post-fabrication selection is demonstrated. This technique reduces the PN by taking advantage of the fact that, when transistor dimensions are reduced, the low-frequency noise and the thermal noise can vary significantly, and the low-frequency noise at the lower end of its distribution is decreased. Using minimum-sized transistors to reduce the impact of low-frequency noise is opposite to the conventional approach of using larger transistors, which relies on averaging the value determined by the PDK model. Applying an intelligent post-fabrication selection process using a genetic algorithm well suited for searching through high-dimensional unstructured spaces to an LC VCO employing the array, the PN at 600-kHz, 1-MHz, and 3-MHz offsets from a 3.8-GHz carrier is lowered by 1.5–2 dB from the average PN and by ∼3.5 dB from the maximum PN. It should be possible to utilize the proposed technique with other PN reduction techniques to realize the ultralow PN oscillators. Finally, it may be possible to increase the operating frequencies of VCOs using the proposed technique, and the investigation of this is an important vector for future research.

ACKNOWLEDGMENT

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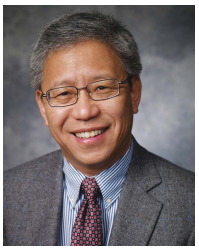

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