1. In the following CMOS active-cascode gain stage, choose a proper identical W/L for M1 and M2 such that the overdrive voltage of M1 is roughly 0.1V. You will also need to choose a proper voltage, $V_{bias}$, to set up the cascode bias for M2 such that $V_o$ is roughly $V_{DD}/2$ or 1.25V. You can assume the booster amplifier is an ideal VCVS with a gain of 20dB. The large resistor (1GΩ) is helpful to bias the gate of M1 in simulation. Tie all transistor bulks to GND. $V_{DD} = 2.5V$. Set all channel lengths in your design to 0.35μm.

![Problem #1 circuit diagram](image)

1) Perform .op analysis and extract all the small-signal parameters of M1 and M2. Are both M1 and M2 in saturation?

2) Calculate the small-signal gain $A_v$ of the amplifier using the s.s. parameters you obtained in 1).

3) Run .dc analysis by sweeping the input $V_i$ or $V_o$ (sweeping $V_o$ needs you to set up the amplifier in a feedback loop). Plot the gain of the amplifier vs. $V_o$ and compare the numerical results of $A_v$ with that obtained in 2).

4) Run .ac analysis with proper setup (AC-coupling the input etc.). Plot the s.s. gain vs. frequency. Compare your results with that of 2).

5) Calculate the output resistance of the amplifier, $R_o$, at the desired operating point.

6) Devise a DC or AC simulation to extract the numerical value of $R_o$ and compare with your hand calculation in 5).

7) How sensitive was the quiescent voltage of $V_o$ to $V_{bias}$? Given the configuration in the diagram, how are the quiescent bias of nodes $V_o$, $X$ (and $V_i$), and $Y$ determined? Can you reason this?
2. In the following resistively loaded MOS differential pair, you are asked to perform DC, AC, and transient simulations to analyze the circuit behavior. Consider using an input common mode (CM) of around VDD/2 or 1.25V. Set the channel length of both M1 and M2 to 0.35μm. In 1) to 7), you can ignore the dashed 10Ohm resistor in the schematic (due to a layout error). In the remaining parts of the problem, you need to include this resistor in your calculations or simulations.

![Problem #2 circuit diagram](image)

1) First, you need to size the W/L of the M1 and M2 to obtain an overdrive voltage of around 0.1V each. You may use a DC sweep to determine the sizing.

2) Once the sizes are chosen, apply a CM voltage of VDD/2 at Vi1 and Vi2. There is no mismatch in the circuit. Do a .op to obtain all s.s. parameters of your devices. Use them to determine the differential mode (DM) s.s. gain (A_{dm}) of your amplifier. Are all transistors biased in saturation?

3) What is the output CM voltage in 2)? Is there any dependence of this on the input CM? if so, explain why and hand calculate the CM gain (A_{cm}) of your amplifier. If not, explain why not.

4) Perform .dc with your amplifier and determine the large-signal transfer characteristic of your amplifier. With your knowledge of the MOS diff. pair and the s.s. parameters from 2), can you sketch the transfer function of the amplifier overlaid on top of the simulation result? Any discrepancies? If so, why?

5) Perform .ac with your amplifier and derive the s.s. gain from simulation result. Does this gain agree with your result from 4)?

6) Perform .tran with your amplifier with a 100mV amplitude sine wave at the frequency of 10MHz. Make sure your CM bias is retained in this simulation. How does the output behave? Perform an FFT on the output waveform and compute the THD of the output.

7) Increase the sinusoidal amplitude to 200mV, 400mV, and 800mV, and observe the output waveform carefully. Summarize your observation and compute the FFT and THD accordingly. Report your THD (considering plotting the THD vs. amplitude).
8) Now consider the 10Ohm resistance shown in the schematic and its effect on the fully differential property of your amplifier. Have the same CM bias on Vi1 and Vi2, perform .op and determine the new set of s.s. parameters.

9) Recalculate the s.s. gains, i.e., \( V_{dm} \), \( V_{cm} \), and devise either DC or AC simulations to determine them. Compare the simulation results with your hand calculations.

10) You will also have \( V_{dm-cm} \) and \( V_{cm-dm} \) due to the imbalance created by the 10Ohm resistor. Can you perform hand calculation to determine these two gains? Also, devise DC or AC simulations for these gains. Compare your simulation results with hand calculations.

11) Can you derive an expression for the input-referred offset of your amplifier? Devise a simulation to corroborate with your calculation.

12) Perform a .tran on the amplifier with the 10Ohm resistor. Use a sinusoidal amplitude of your choice. How can you conclude about the distortion produced by the imbalance?

Notes on Report and Simulation Results

Type your report, calculation and simulation results. Annotate your plots properly for clarity.

You are encouraged to work in a group of two (and no more than two) and submit a joint report/design. Discussion with others in class is encouraged. However, please submit a genuine design. No exchange of SPICE decks or schematics.