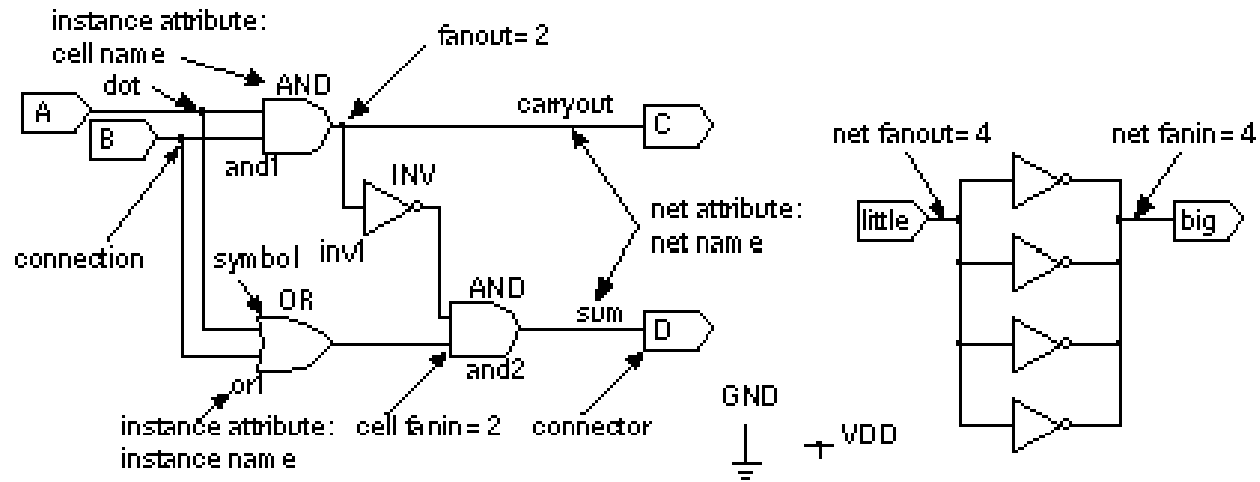


LOW-LEVEL DESIGN ENTRY

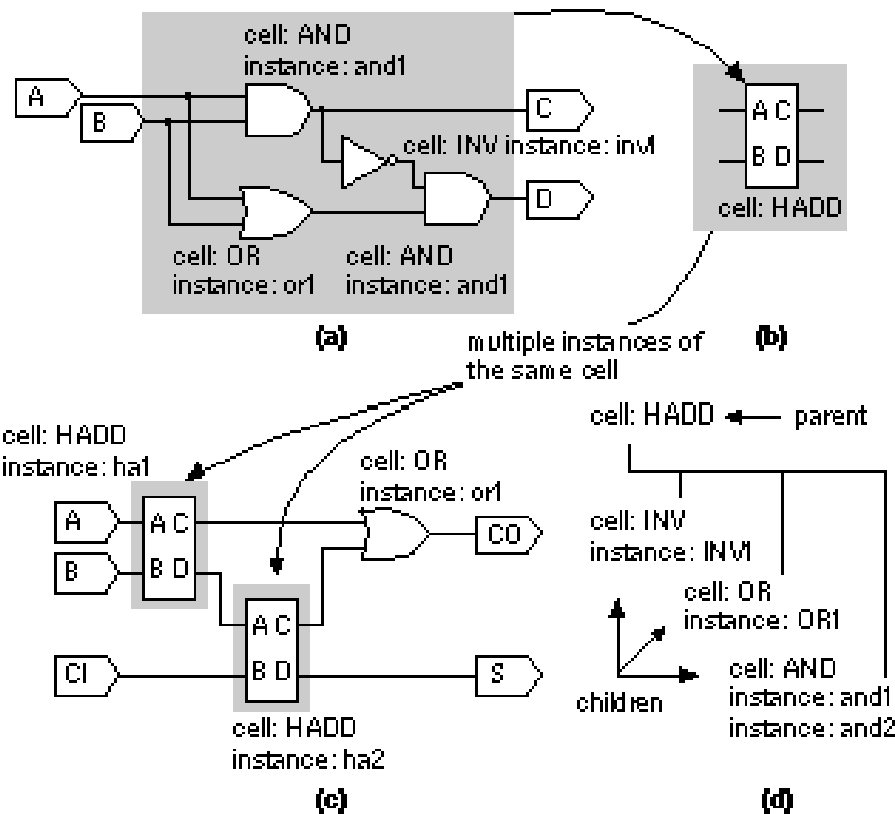
- Design Entry - Description of a microelectronic system to a set of EDA (Electronic Design Automation) tools
- Representation by schematic entry
- Output of schematic entry tools is a 'netlist' file containing detailed description of all the components in a system and their interconnections
- HDLs for design entry allow generation of netlist directly using logic synthesis

Schematic Entry



Terms used in circuit schematics

Hierarchical Design



- (a) The schematic of a half-adder, the subschematic of cell HADD
- (b) A schematic symbol for the half adder
- (c) A schematic that uses the half-adder cell
- (d) The hierarchy of cell HADD

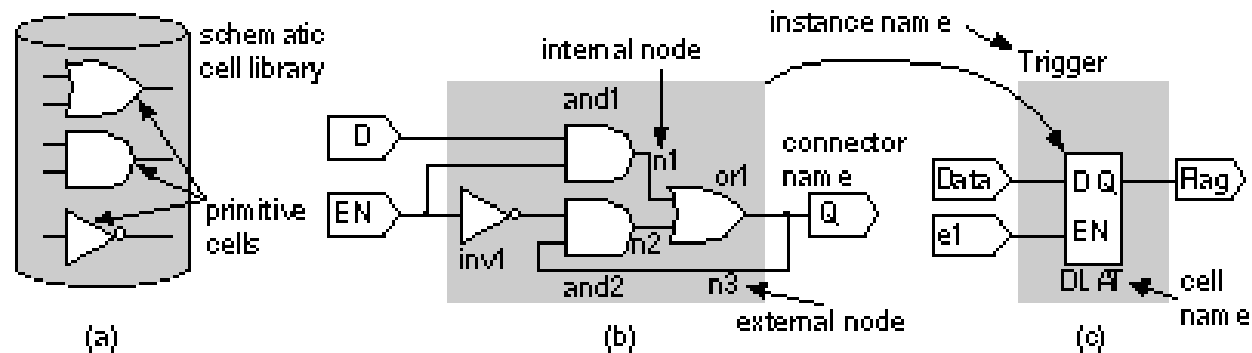
The Cell Library

- Library elements - cells or modules
- Schematic libraries - not flexible, vendor dependent, porting issues
- Hard Macro - placement information, relative location within the macro is fixed
- Soft Macro - Interconnection information, can be varied

Names

- cell name - identifier for each of the cells in an ASIC schematic
- cell instance - reference to the primitive cell
- instance name - for the cell instance used
- icon (symbol) - pictorial representation of a cell

Schematic Icons and Symbols



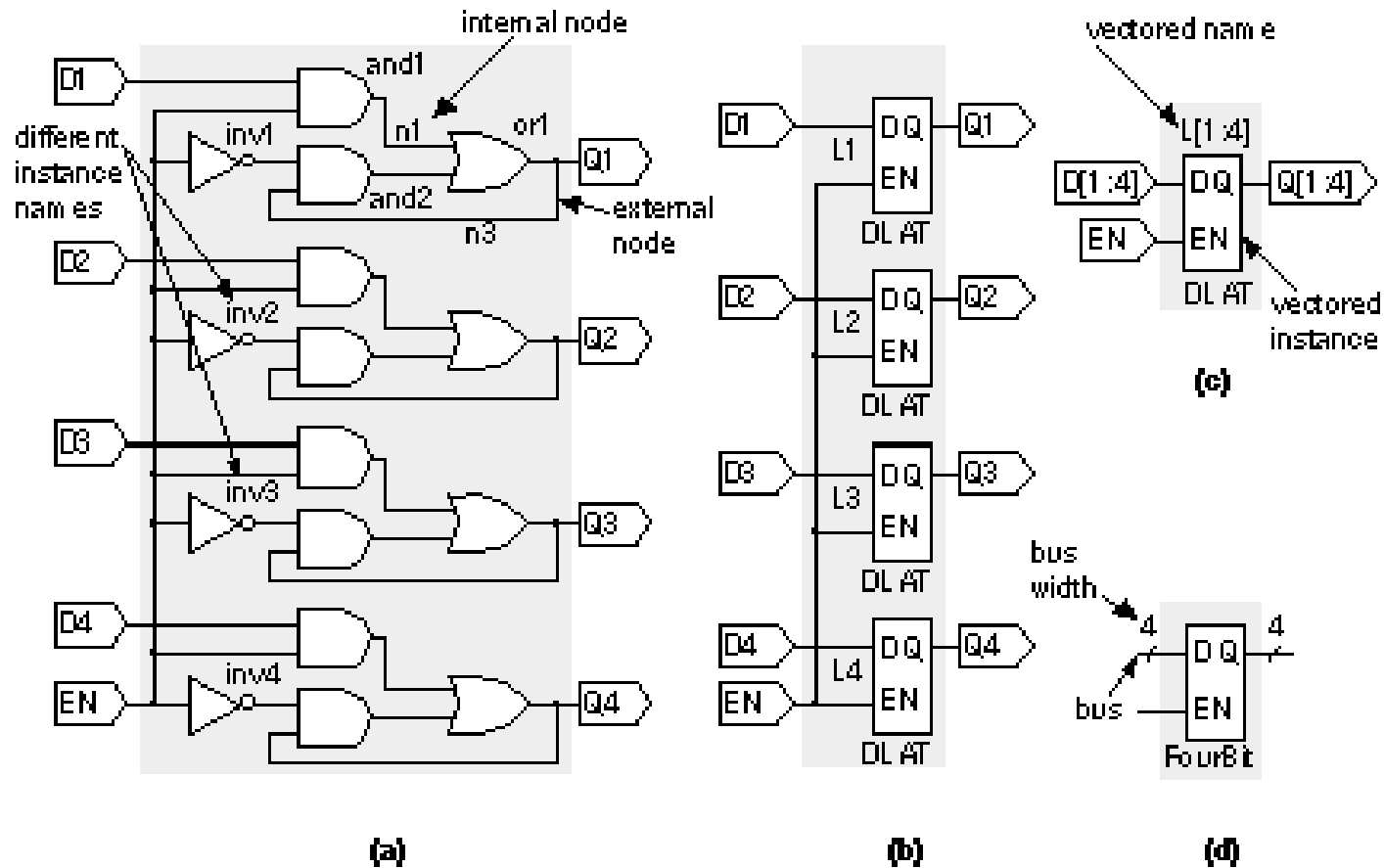
A cell and its subschematic

(a) A schematic library containing icons for the primitive cells

(b) A subschematic for a cell, DLAT, showing the instance names for the primitive cells

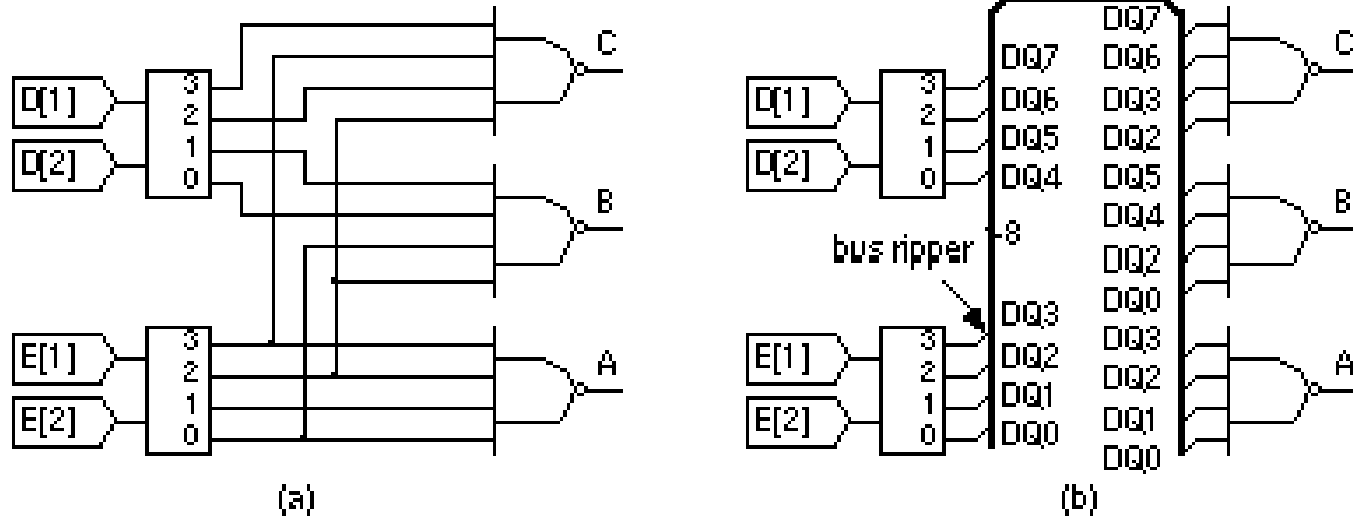
(c) A symbol for cell DLAT

A 4-bit latch



- (a) drawn as a flat schematic from gate-level primitives
- (b) drawn as four instances of the cell symbol DLAT
- (c) drawn using a vectored instance of the DLAT cell symbol with cardinality of 4
- (d) drawn using a new cell symbol with cell name FourBit

Connections

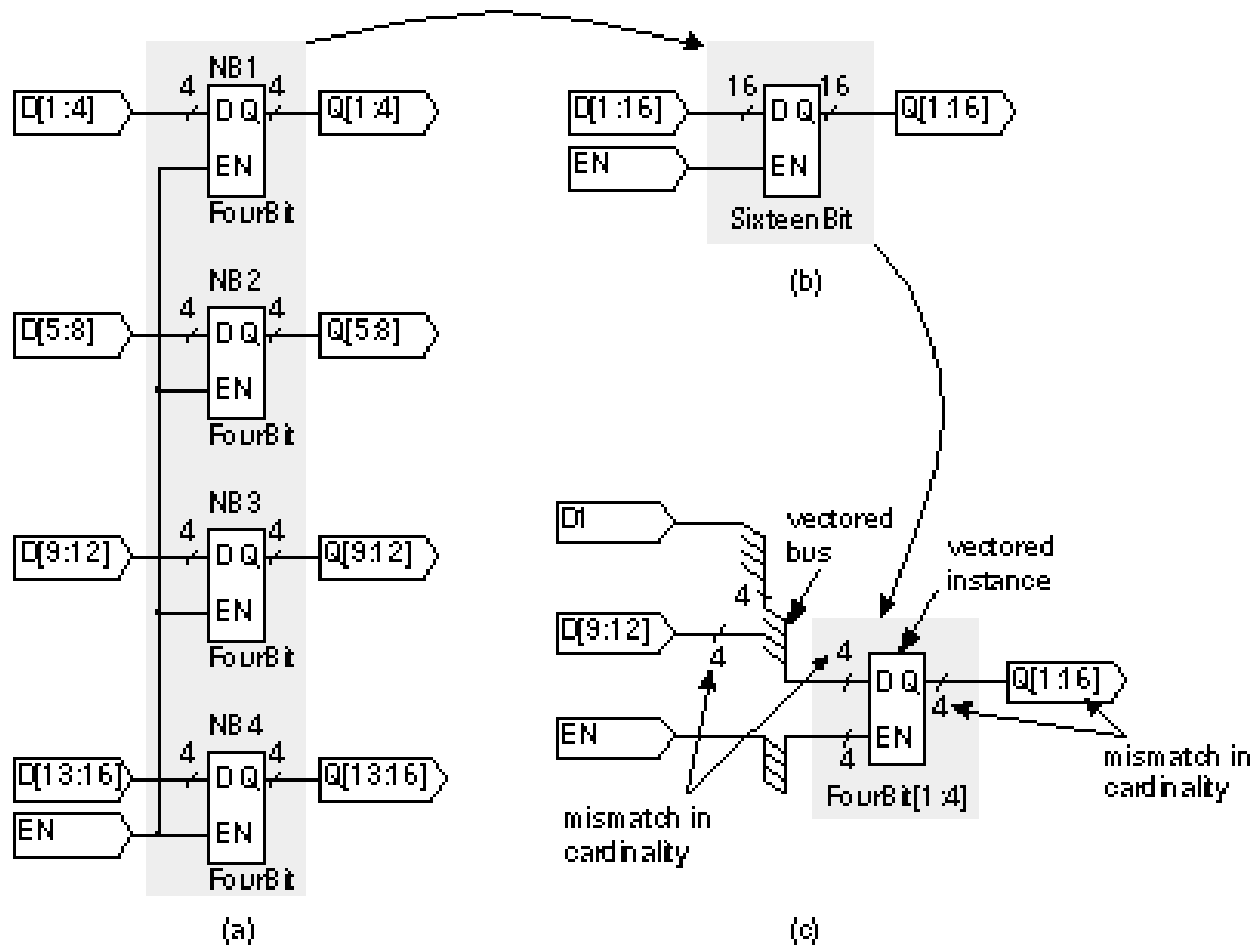


An example of the use of a bus to simplify a schematic

(a) An address decoder without using a bus

(b) A bus with bus rippers simplifies the schematic and reduces the possibility of making a mistake in creating and reading the schematic

Vectored Instances and Buses



Netlist Screener

typical features provided by a Netlist Screener

- schematic or netlist screener catches errors at an early stage
- handle (to find components)
- snap to grid
- wildcard matching
- automatic naming
- datapath (multiple instances)
- vectored cell instance
- vectored instance
- cell cardinality • cardinality
- terminal polarity • terminal direction
- fanout • fanin
- standard load

Low-Level Design Languages

ABEL - PLD programming language from Data I/O

CUPL - PLD programming language from Logical Devices

PALASM - PLD programming language from AMD/MMI

PLA Tools

EDIF - Electronic Design Interchange Format for exchanging information
between EDA tools