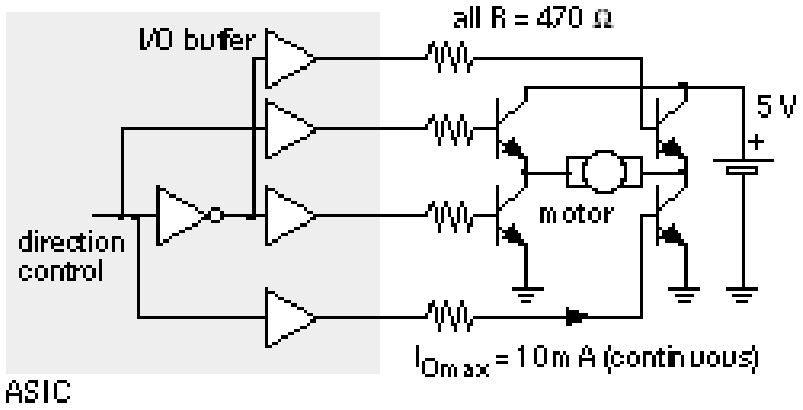
PROGRAMMABLE ASIC I/O CELLS

Types of I/O requirements

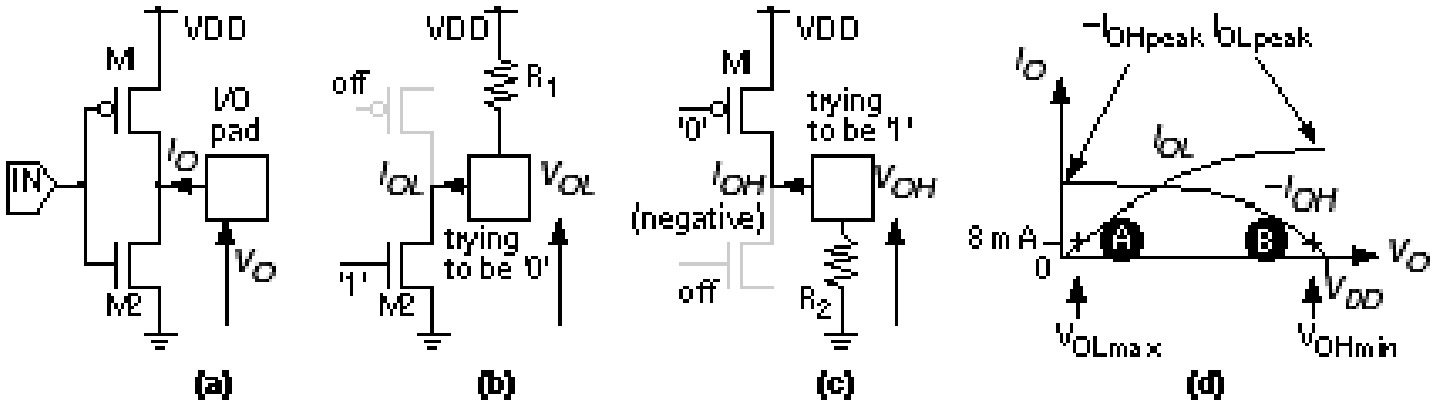
- DC Output
- AC Output
- DC Input
- AC Input
- Clock Input
- Power Input

DC Output



A circuit to drive a small electric motor (0.5 A) using ASIC I/O buffers

CMOS output buffer characteristics



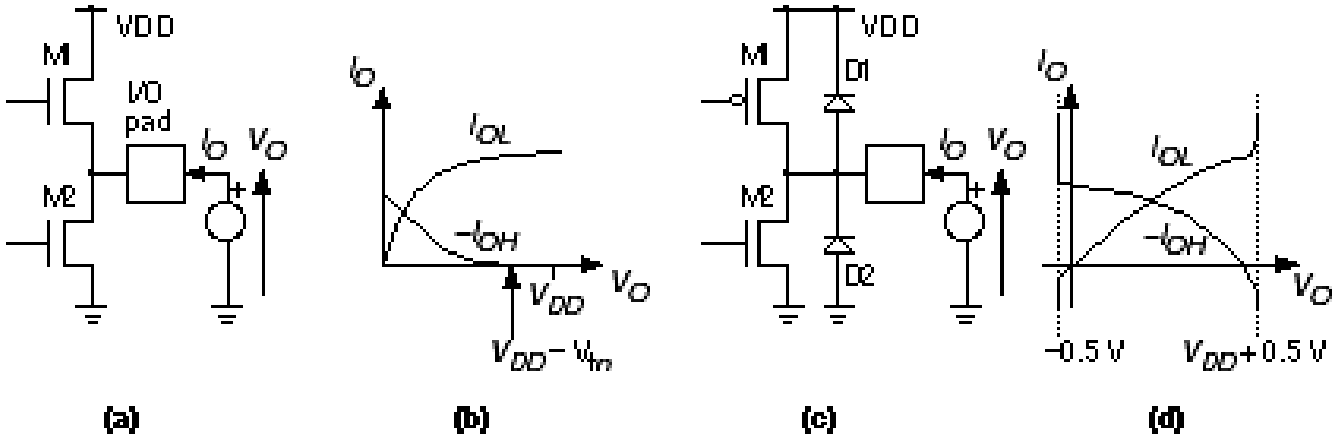
(a) A CMOS complementary output buffer

(b) Transistor M2 (M1 off) sinks (to GND) a current I OL through a pull-up resistor, R 1

(c) Transistor M1 (M2 off) sources (from VDD) a current –I OH (I OH is negative) through a pull-down resistor, R 2

(d) Output characteristics:

Totem-Pole Output



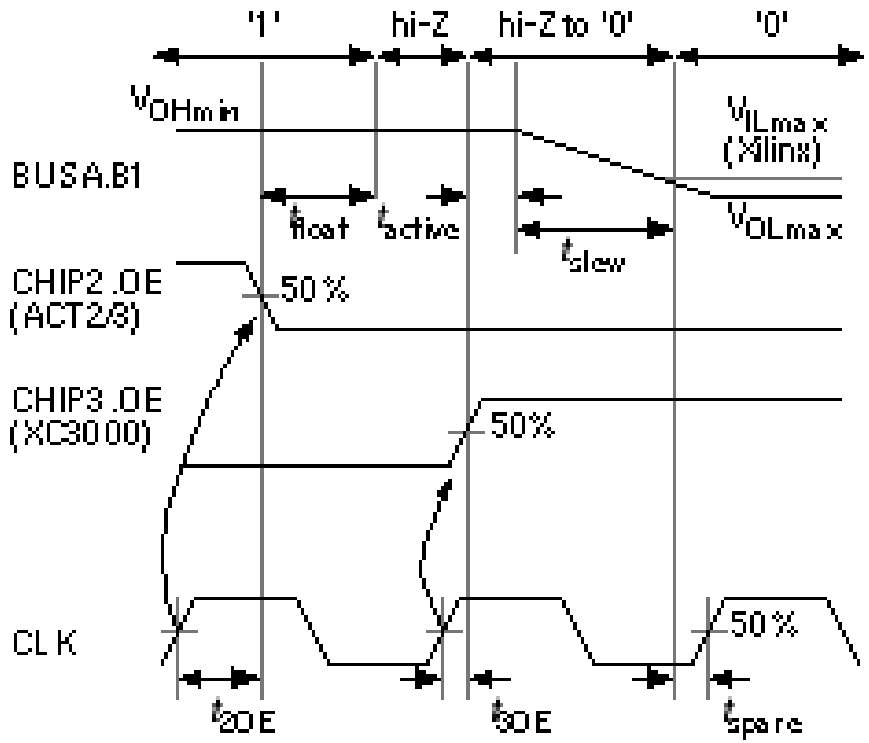
(a) A CMOS totem-pole output stage (both M1 and M2 are n -channel transistors)

(b) Totem-pole output characteristics (notice the reduced signal swing)

(c) Clamp diodes, D1 and D2, in an output buffer (totem-pole or complementary) prevent the I/O pad from voltage excursions greater than V_{DD} and less than V_{SS}

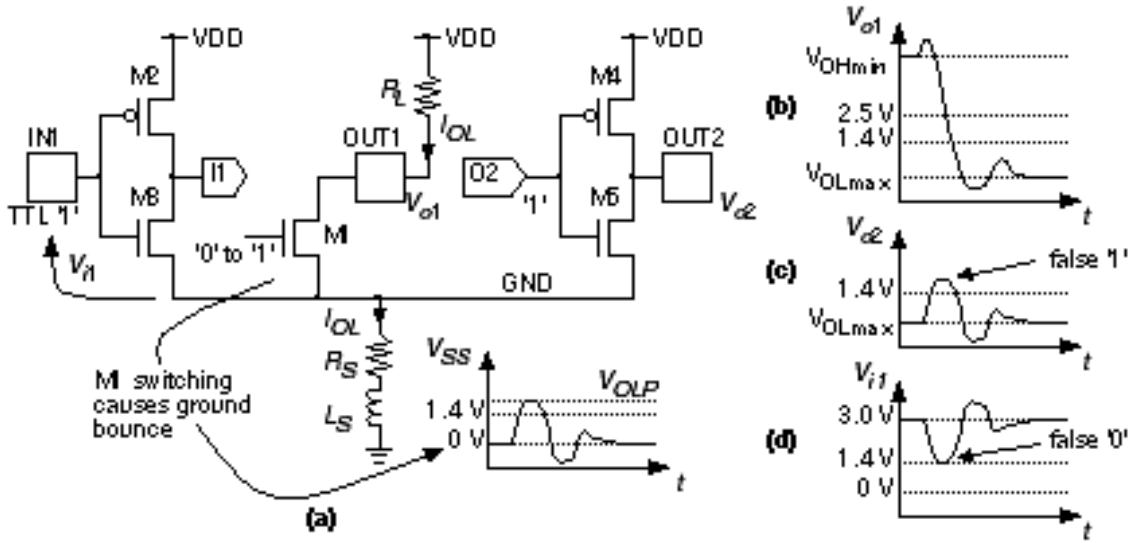
(d) The clamp diodes conduct as the output voltage exceeds the supply voltage bounds

AC Output



Three-state bus timing

Supply Bounce



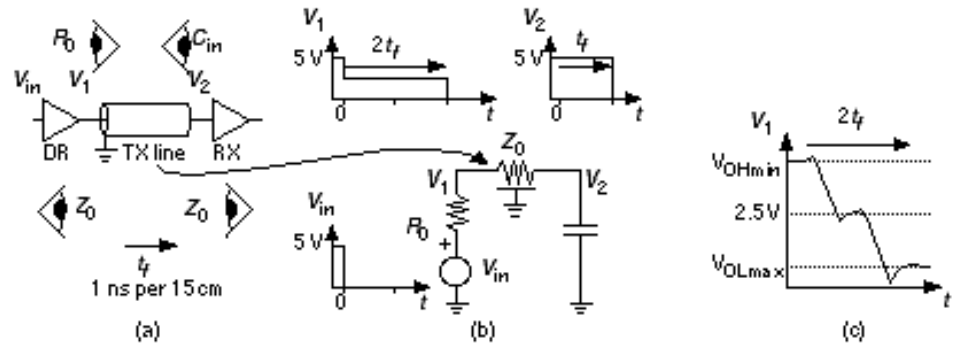
(a) As the pull-down device, M1, switches, it causes the GND net (value V ss) to bounce

(b) The supply bounce is dependent on the output slew rate

(c) Ground bounce can cause other output buffers to generate a logic glitch

(d) Bounce can also cause errors on other inputs

Transmission Lines



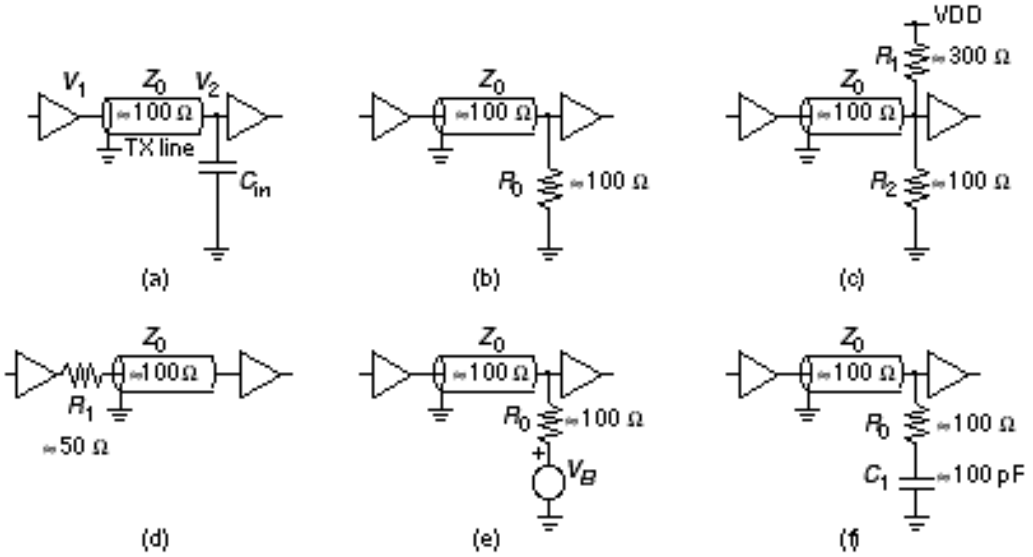
(a) A printed-circuit board (PCB) trace is a transmission (TX) line

(b) A driver launches an incident wave, which is reflected at the end of the line

(c) A connection starts to look like a TX line when the rise time is about

2 times line delay (2 t f)

Transmission line termination



(a) Open-circuit or capacitive termination

(b) Parallel resistive termination

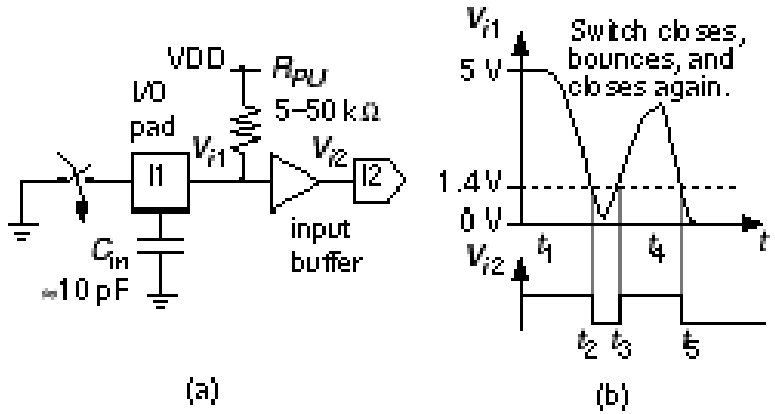
(c) Thévenin termination

(d) Series termination at the source

(e) Parallel termination using a voltage bias

(f) Parallel termination with a series capacitor

DC Input



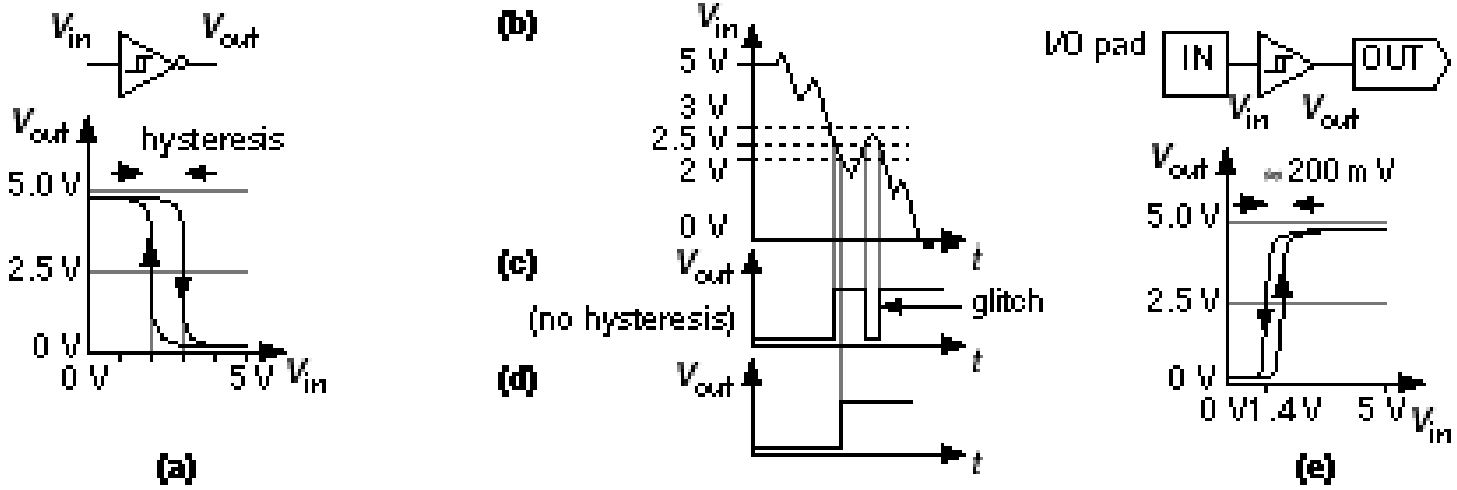
Switch input

(a) A pushbutton switch connected to an input buffer with a pull-up resistor

(b) As the switch bounces several pulses may be generated

Signal debounced using a SR flip-flop or a state machine

DC input



(a) A Schmitt-trigger inverter • lower switching threshold • upper switching threshold • difference between thresholds is the hysteresis

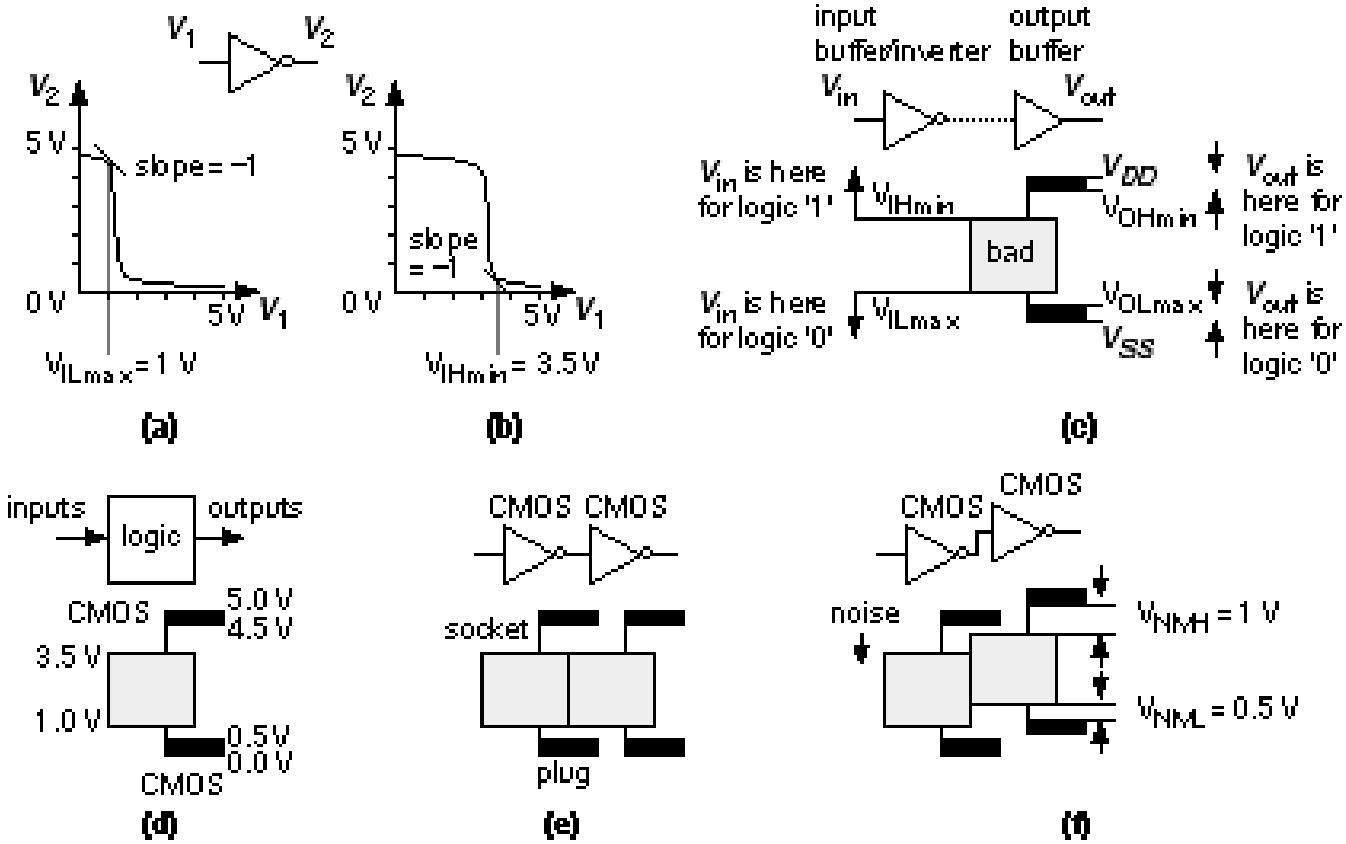
(b) A noisy input signal

(c) Output from an inverter with no hysteresis

(d) Hysteresis helps prevent glitches

(e) A typical FPGA input buffer with a hysteresis of 200 mV and a threshold of 1.4 V

Noise Margins



(a) Transfer characteristics of a CMOS inverter with the lowest switching threshold

(b) The highest switching threshold

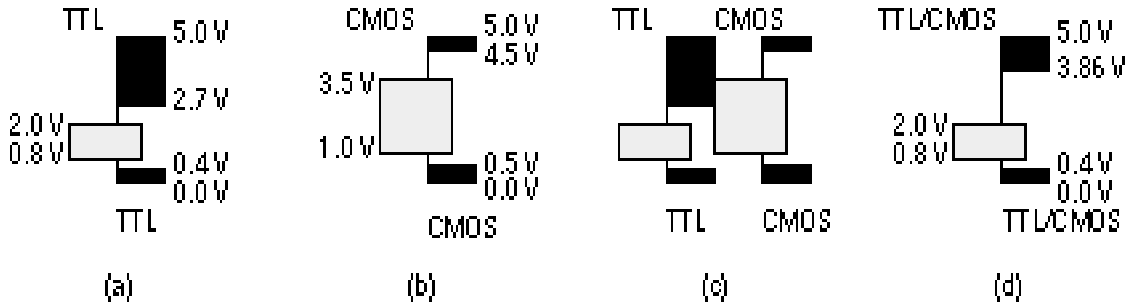
(c) A graphical representation of CMOS logic thresholds

(d) Logic thresholds at the inputs and outputs of a logic gate or an ASIC

(e) The switching thresholds viewed as a plug and socket

(f) CMOS plugs fit CMOS sockets and the clearances are the noise margins

TTL and CMOS logic thresholds



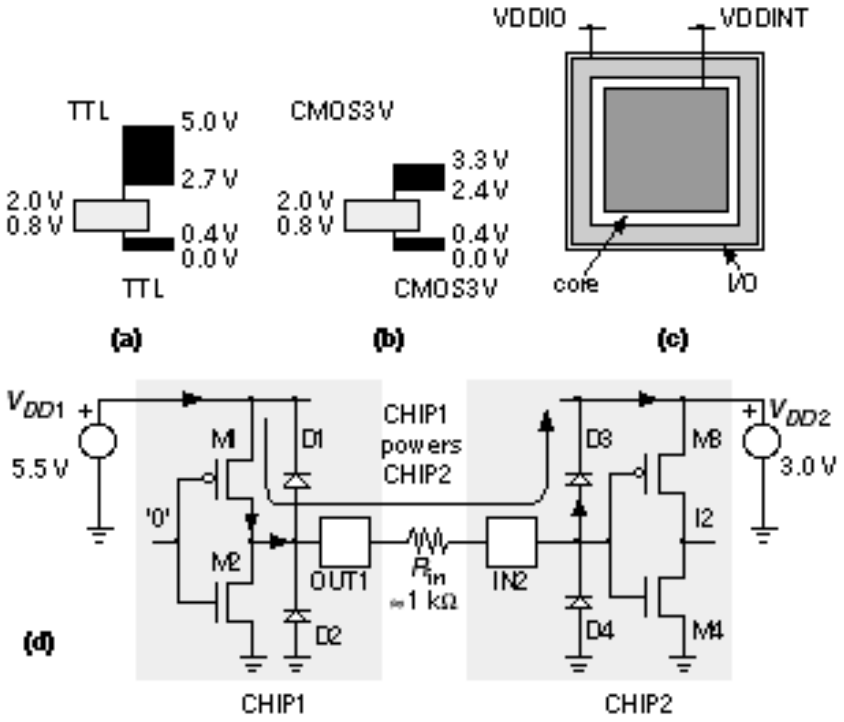
(a) TTL logic thresholds

(b) Typical CMOS logic thresholds

(c) A TTL plug will not fit in a CMOS socket

(d) Raising V_{OHmin} solves the problem

Mixed-voltage systems



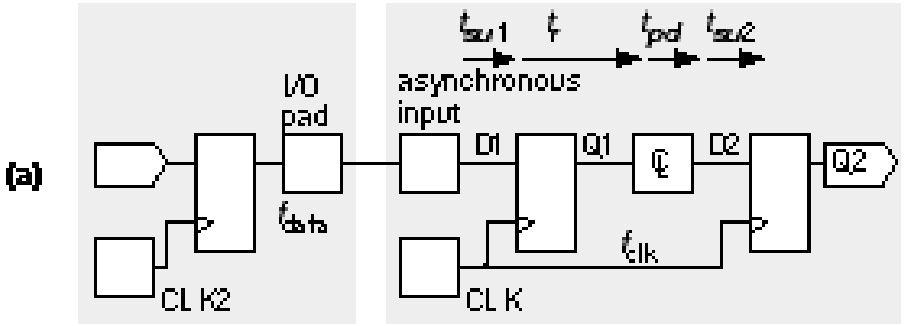
(a) TTL levels

(b) Low-voltage CMOS levels • JEDEC 8 • 3.3 ± 0.3 V

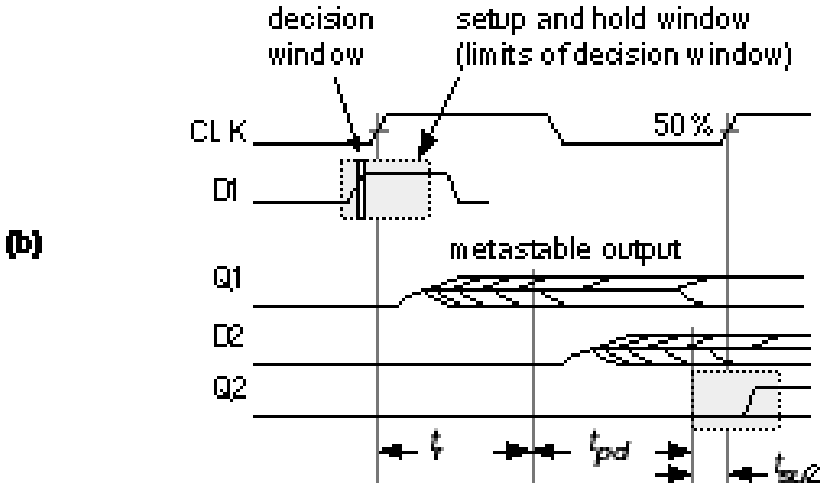
(c) Mixed-voltage ASIC • 5 V-tolerant I/O • V_{DDint} and $V_{DDI/O}$

(d) A problem when connecting two chips with different supply voltages—caused by the input clamp diodes

Metastability



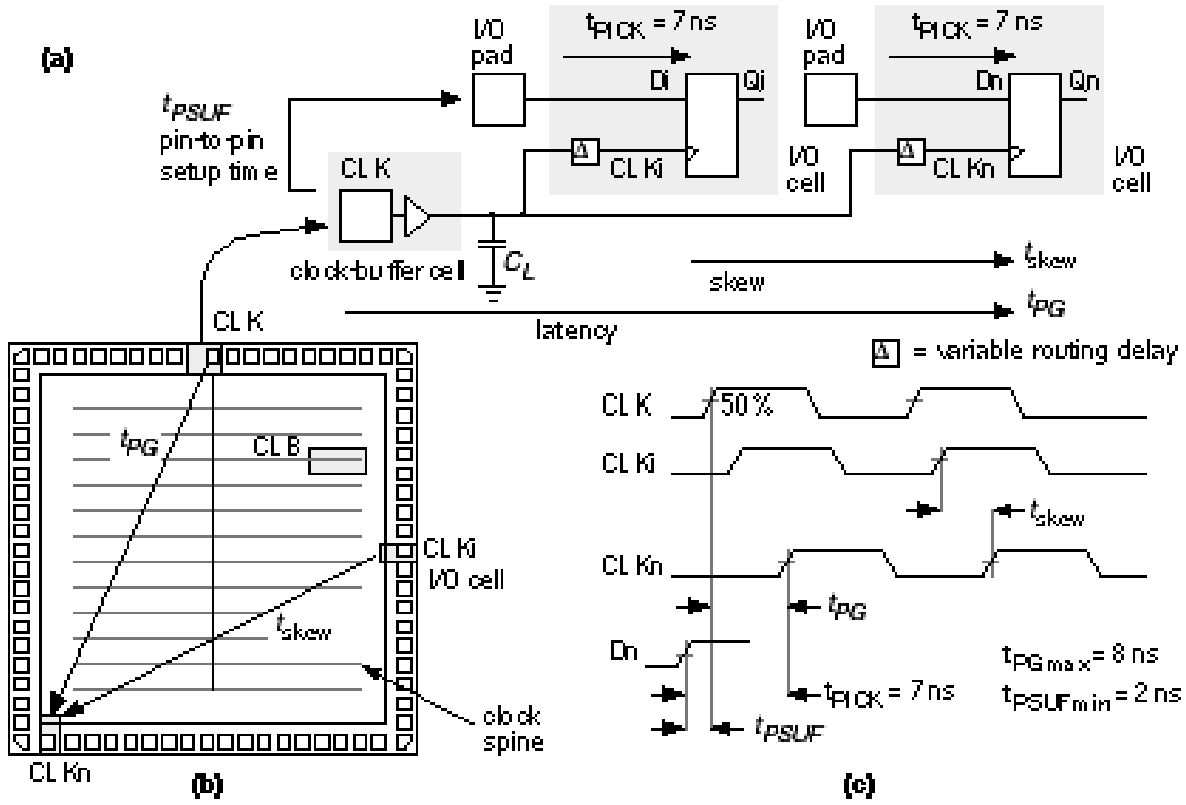
Data coming from one clocked system is an asynchronous input to another



A flip-flop (or latch, a sampler) has a very narrow decision window bounded by the setup and hold times to resolve the input

If the data input changes inside the decision window (a setup or hold-time violation) the output may be metastable —neither '1' or '0'—an upset

Clock Input

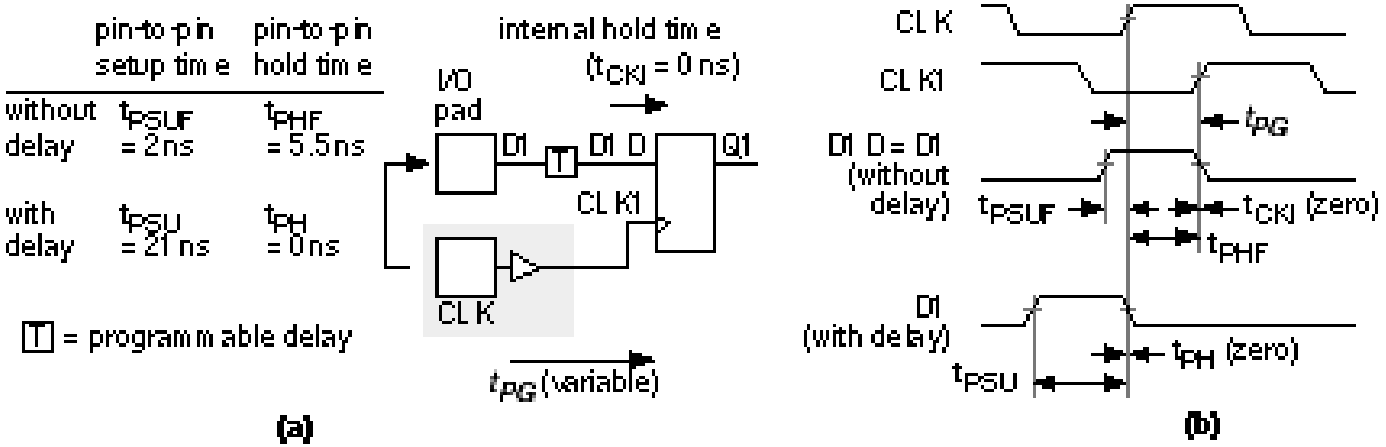


(a) Timing model (Xilinx XC4005-6)

(b) A simplified view of clock distribution • clock skew • clock latency

(c) Timing diagram

Registered Input



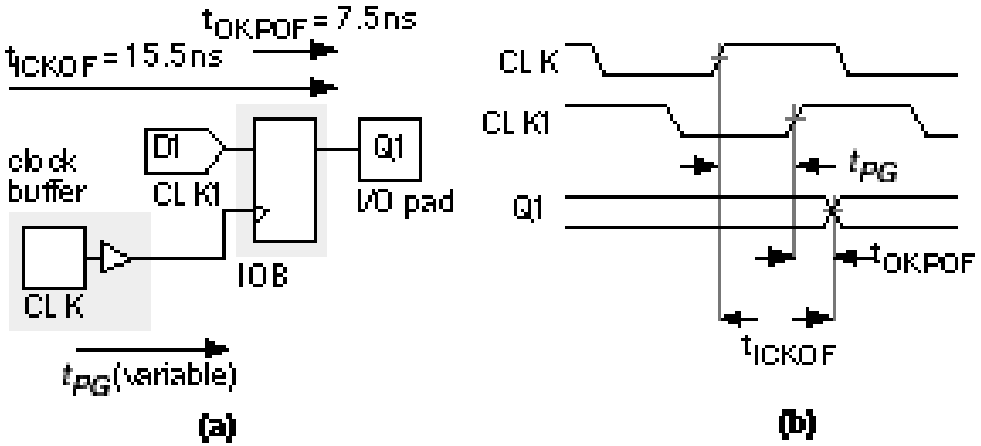
Programmable input delay

(a) Pin-to-pin timing model (XC4005-6) with pin-to-pin timing parameters

(b) Timing diagrams with and without programmable delay

Notice $t_{PSUFmin}$ = 2 ns " $t_{PICK} – t_{PGmax}$ = –1 ns

Registered output



(a) Timing model with values for an XC4005-6 programmed with the fast slew-rate option

(b) Timing diagram

Xilinx I/O Block