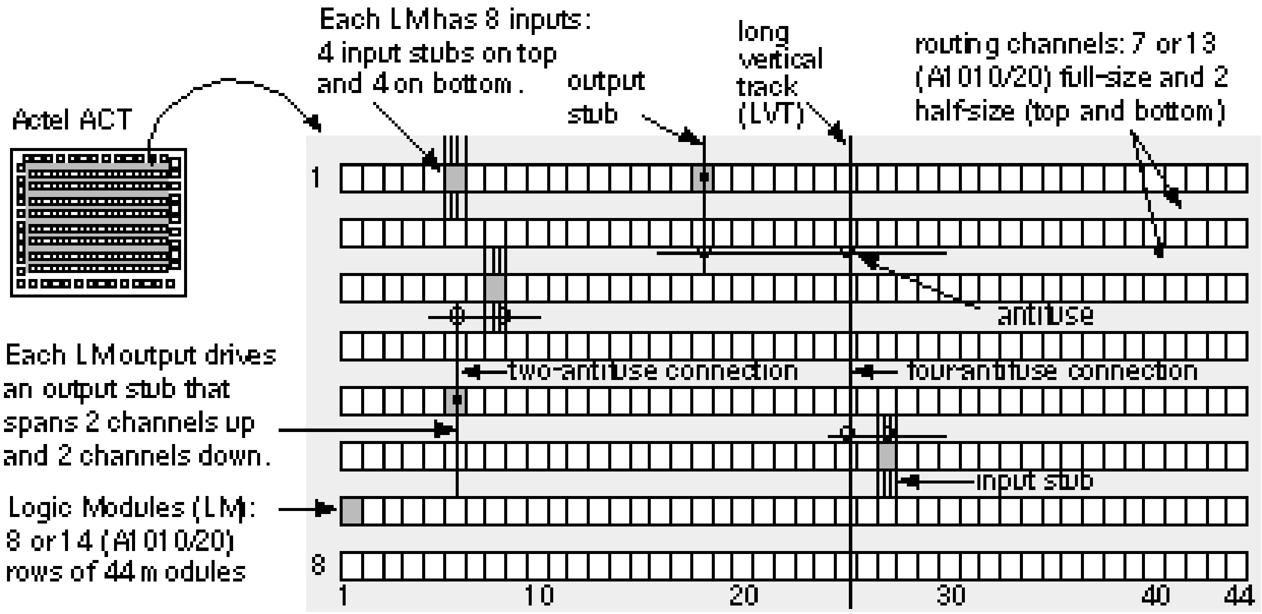
PROGRAMMABLE ASIC INTERCONNECT

- The structure and complexity of the interconnect is largely determined by the programming technology and the architecture of the basic logic cell
- The first programmable ASICs were constructed using two layers of metal; newer programmable ASICs use three or more layers of metal interconnect.

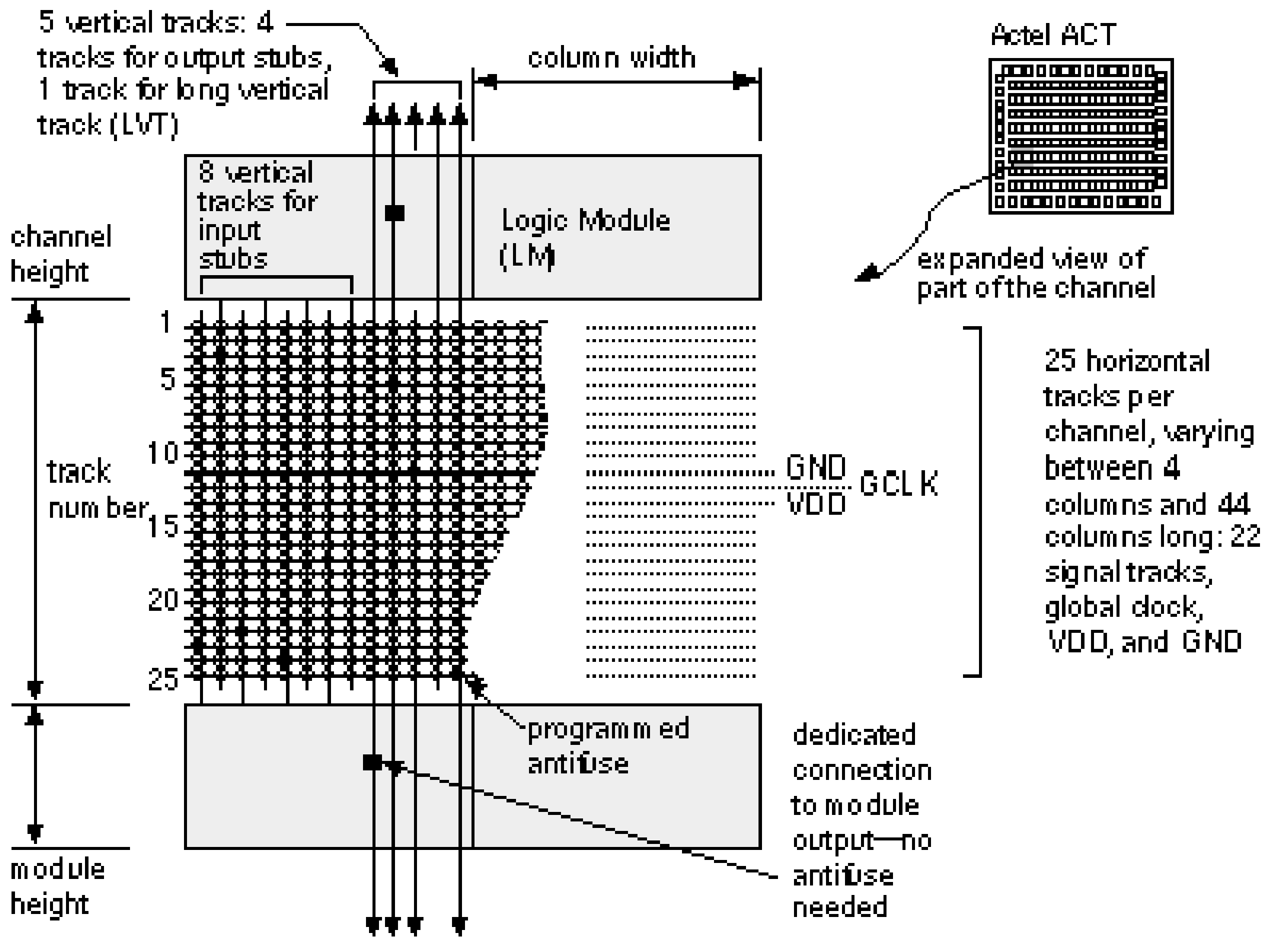
Actel ACT



The Actel ACT family interconnect scheme shown is similar to a channeled gate array

- The channel routing uses dedicated rectangular areas of fixed size within the chip called wiring channels
- Within the horizontal or vertical channels wires run horizontally or vertically, respectively, within tracks
- Actel divides the fixed interconnect wires within each channel into various lengths or wire segments
- The designer then programs the interconnections by blowing antifuses and making connections between wire segments

ACT 1 horizontal and vertical channel architecture. (Source: Actel.)

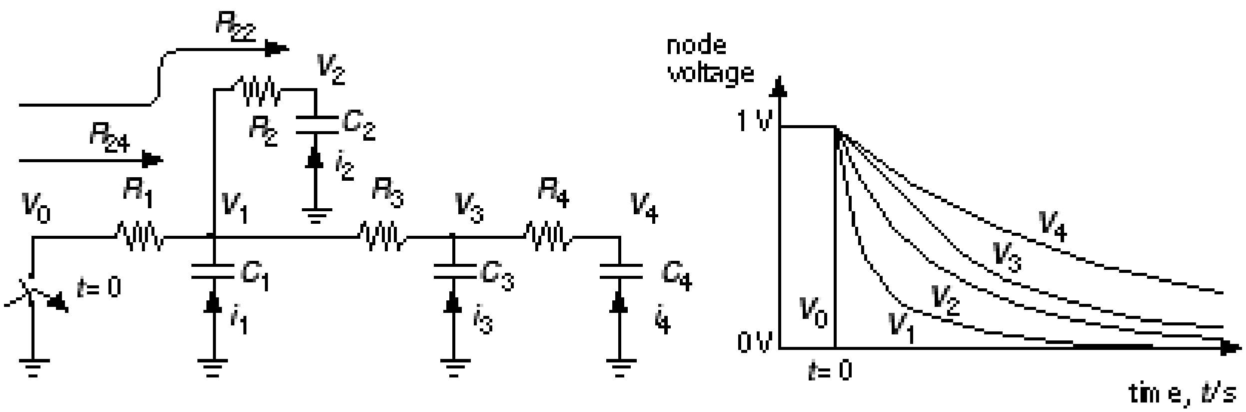


Routing Resources

- 22 horizontal tracks per channel for signal routing with three tracks dedicated to VDD, GND and the global clock (GCLK)
- Eight vertical tracks per Logic Module are available for inputs
- A vertical track that extends across the two channels above the module and across the two channels below the module - Output Stub
- One vertical track per column is a long vertical track (LVT) that spans the entire height of the chip

Elmore’s Constant

- Aims at analysis of RC networks to examine the delays due to interconnects



(a) (b)

RC tree —representing a net with a fanout of two

The waveforms as a result of closing the switch at t = 0

$$V_i(t) = \exp(-t/\tau_{Di});\ \tau_{Di} = \sum_{k=1}^{n} R_{ki} C_k$$

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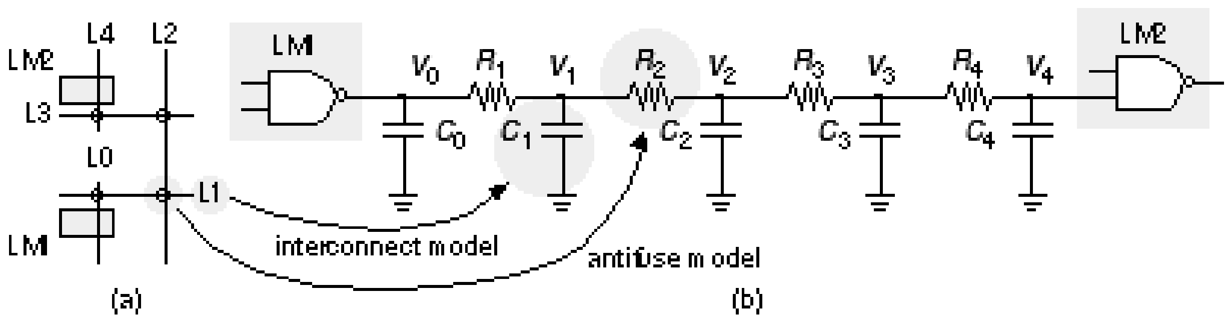
τ_{Di} - Elmore delay

different for each node

RC Delay in Antifuse Connections



Actel routing model

(a) A four-antifuse connection. L0 is an output stub, L1 and L3 are horizontal tracks, L2 is a long vertical track (LVT), and L4 is an input stub

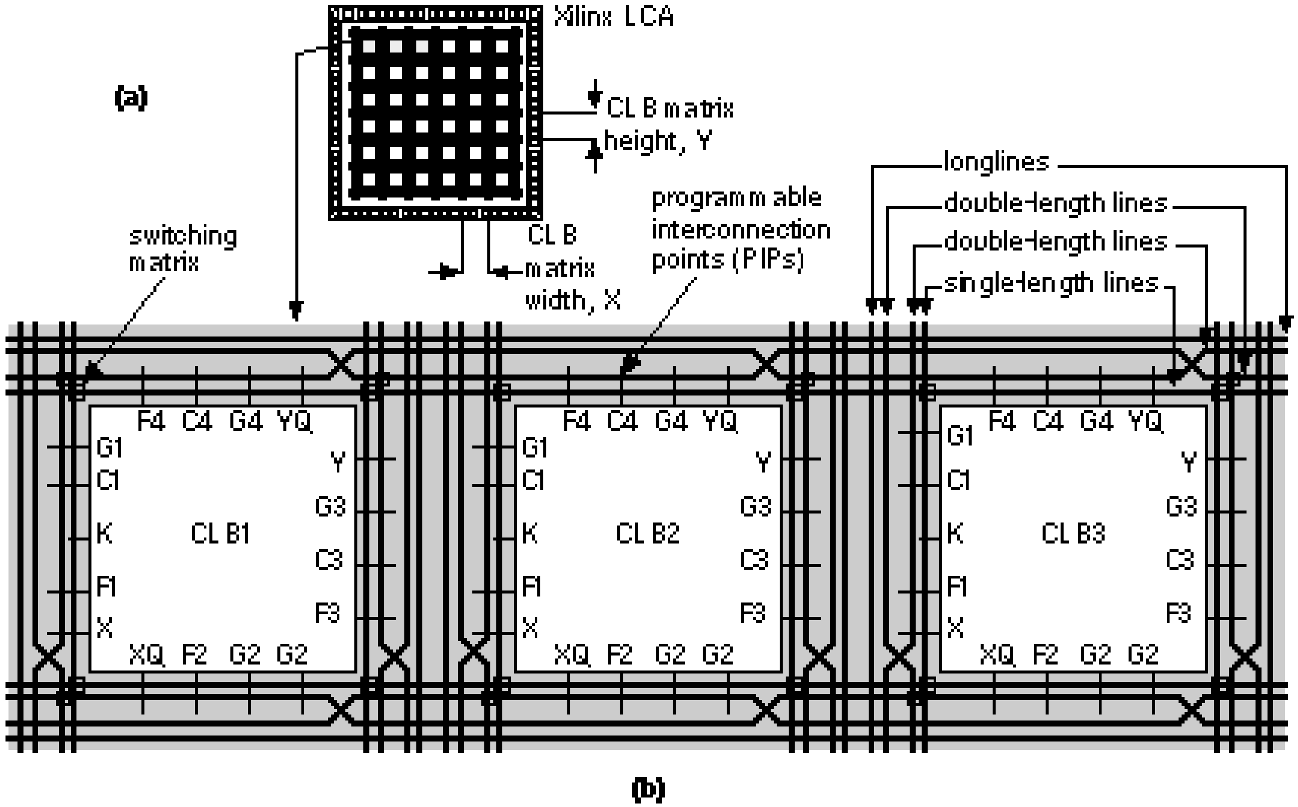
(b) An RC-tree model. Each antifuse is modeled by a resistance and each interconnect segment is modeled by a capacitance

$$\tau_{D4} = R_{14}C_1 + R_{24}C_2 + R_{14}C_1 + R_{44}C_4$$

$$= (R_1 + R_2 + R_3 + R_4)C_4 + (R_1 + R_2 + R_3)C_3 + (R_1 + R_2)C_2 + R_1C_1$$

- Two antifuses will generate a 3 RC time constant
- Three antifuses a 6 RC time constant
- Four antifuses gives a 10 RC time constant
- Interconnect delay grows quadratically ($x\ n^2$) as we increase the interconnect length and the number of antifuses, n

Xilinx LCA



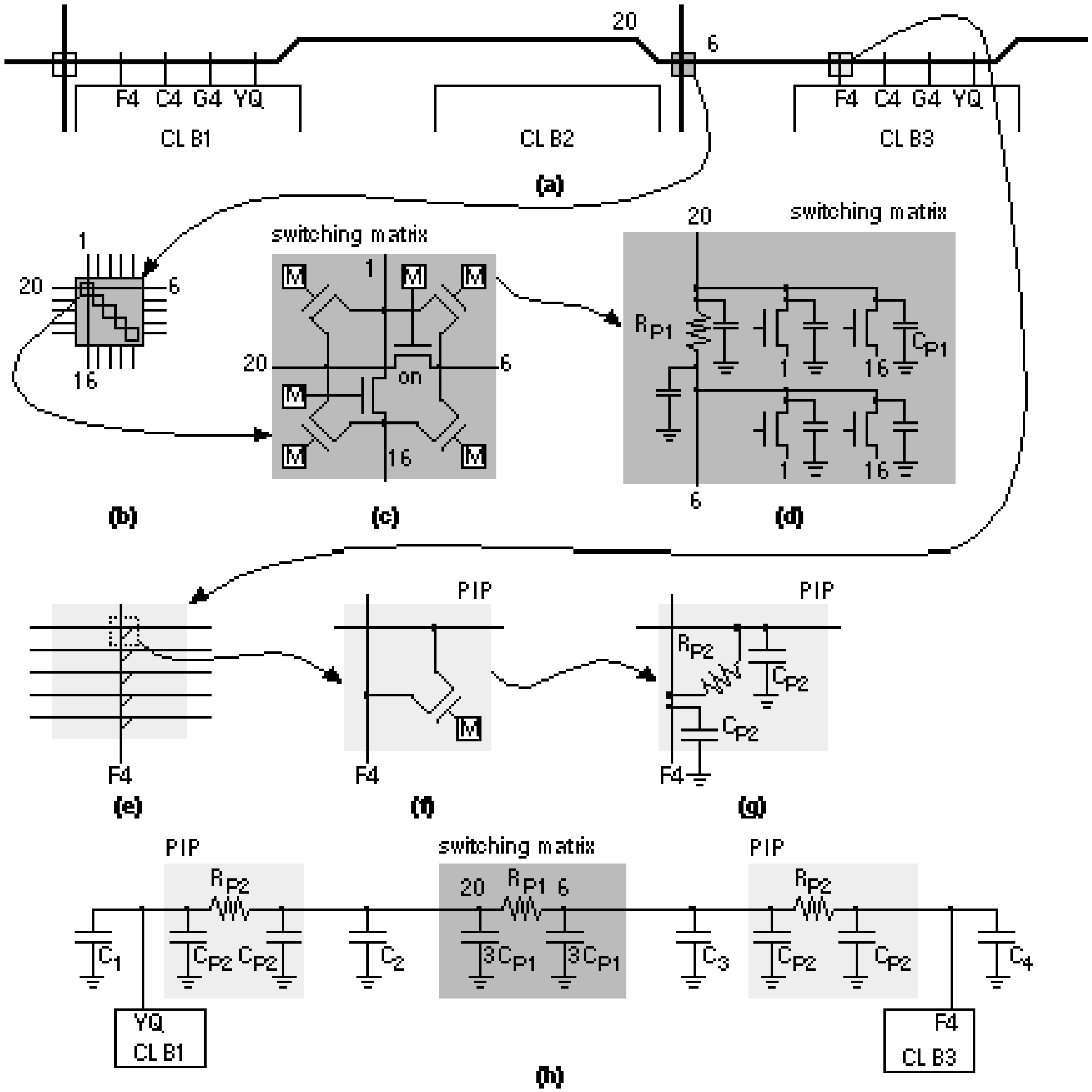
Xilinx LCA interconnect

(a) The LCA architecture (notice the matrix element size is larger than a CLB)

(b) A simplified representation of the interconnect resources. Each of the lines is a bus.

- The vertical lines and horizontal lines run between CLBs.
- The general-purpose interconnect joins switch boxes (also known as magic boxes or switching matrices).
- The long lines run across the entire chip. It is possible to form internal buses using long lines and the three-state buffers that are next to each CLB.
- The direct connections (not used on the XC4000) bypass the switch matrices and directly connect adjacent CLBs.
- The Programmable Interconnection Points (PIP s) are programmable pass transistors that connect the CLB inputs and outputs to the routing network.
- The bi-directional (BIDI) interconnect buffers restore the logic level and logic strength on long interconnect paths

Interconnect delay in a Xilinx LCA array



(a) A portion of the interconnect around the CLBs

(b) A switching matrix

(c) A detailed view inside the switching matrix showing the pass-transistor arrangement

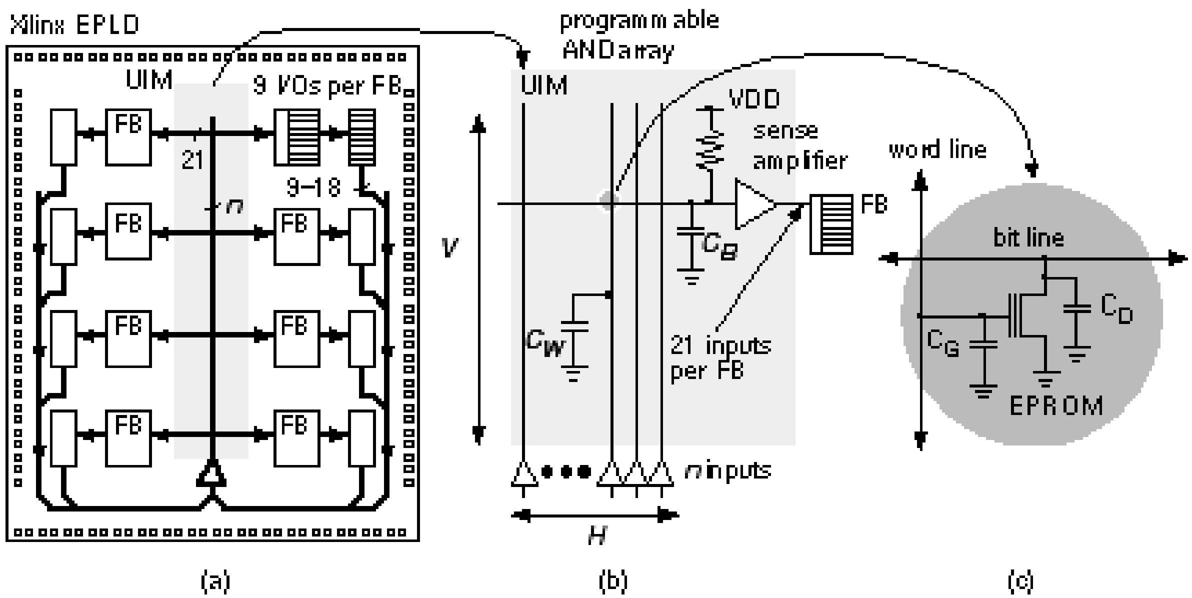
(d) The equivalent circuit for the connection between nets 6 and 20 using the matrix

(e) A view of the interconnect at a Programmable Interconnection Point (PIP)

(f) and (g) The equivalent schematic of a PIP connection

(h) The complete RC delay path

Xilinx EPLD



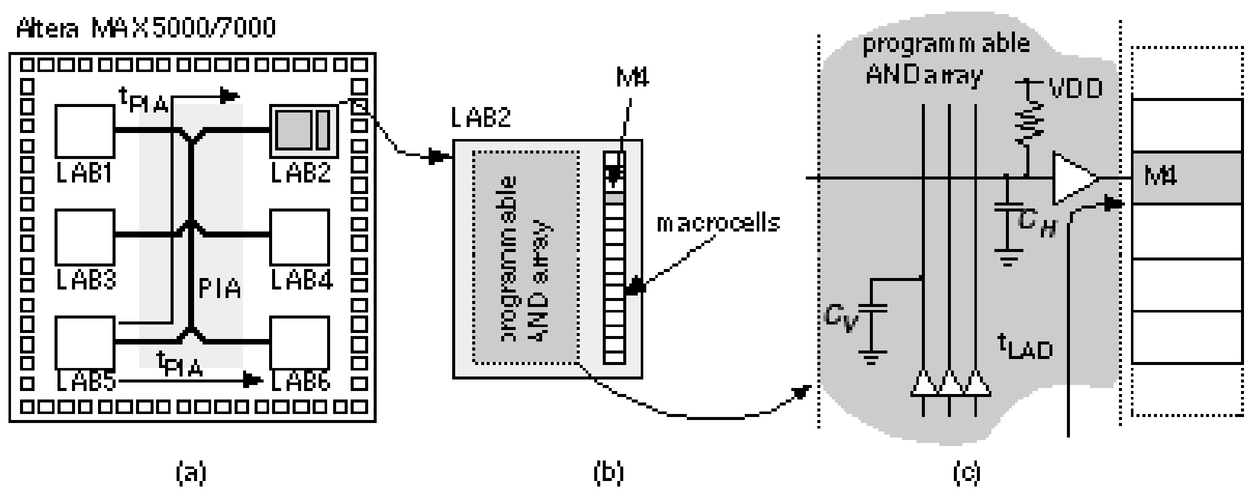
The Xilinx EPLD UIM (Universal Interconnection Module)

(a) A simplified block diagram of the UIM. The UIM bus width, n , varies from 68 (XC7236) to 198 (XC73108)

(b) The UIM is actually a large programmable AND array

(c) The parasitic capacitance of the EPROM cell

Altera MAX 5000 and 7000



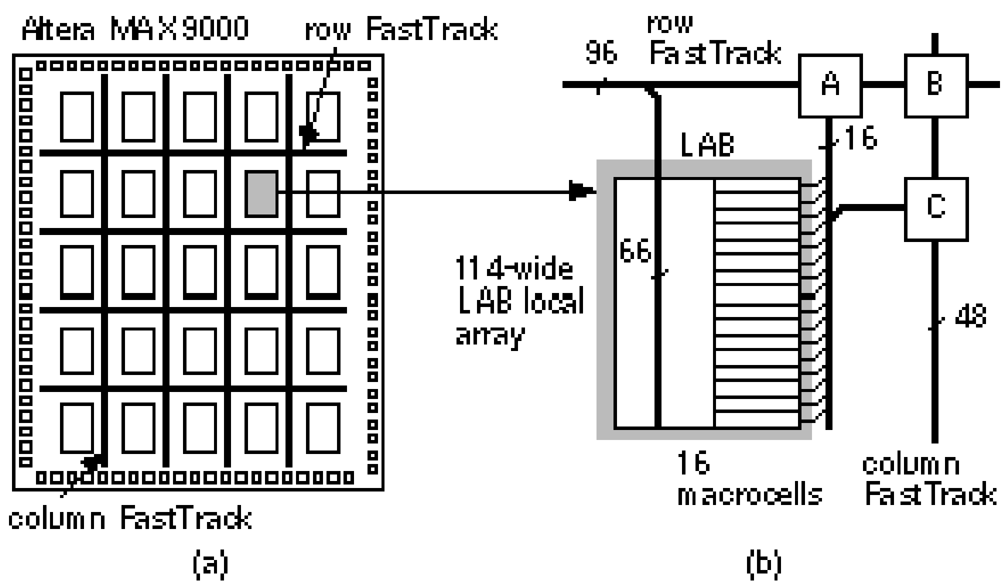
Altera MAX interconnect scheme

(a) The PIA (Programmable Interconnect Array) is deterministic—delay is independent of the path length

(b) Each LAB (Logic Array Block) contains a programmable AND array

(c) Interconnect timing within a LAB is also fixed

Altera MAX 9000

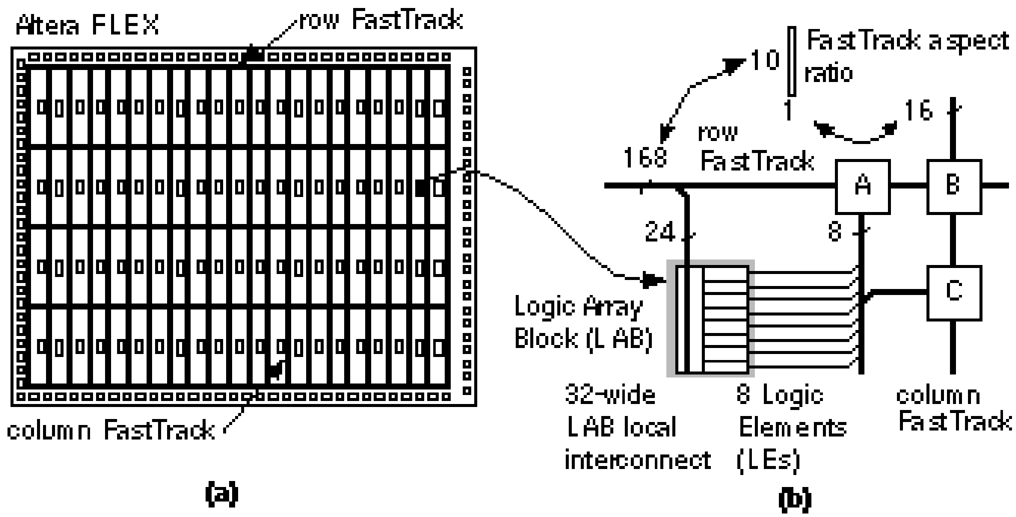


Altera MAX 9000 interconnect scheme

(a) A 4 x 5 array of Logic Array Blocks (LABs), the same size as the EMP9400 chip

(b) A simplified block diagram of the interconnect architecture showing the connection of the FastTrack buses to a LAB

Altera FLEX



Altera FLEX interconnect scheme

(a) The row and column FastTrack interconnect. The chip shown, with 4 rows x 21 columns, is the same size as the EPF8820

(b) A simplified diagram of the interconnect architecture showing the connections between the FastTrack buses and a LAB. Boxes A, B, and C represent the bus-to-bus connections