EE 3111 – Lab 7.2

FET Amplifiers
FET Amplifier

- Device/circuit that alters the amplitude of a signal, while keeping input waveform shape
- FET amplifiers run the FET in active/saturation mode. The **drain current** is determined by small **input voltage**
  - FET amplifier does not have a β, it has transconductance \( g_m \)
- Output voltage is determined by input, \( g_m \), and circuit
- The BJT amplifiers we studied have FET equivalents
Can build common gate, common source or common drain amplifiers
We have two common source, one common drain and one common gate here
Different configurations have different gains and input/output impedance
Input and output impedance can be very important depending on application!

 BJT Amplifier

VDD=10Vdc
RD
10K
2N5485
Function Generator

VDD=10Vdc
RD
10K
2N5485
Function Generator

VDD=10V
2N5485
Function Generator

VDD=10V
RD
10K
RS
10K
2N5485
Function Generator

Function Generator
FET Model

- Active mode, low-frequency model
- $g_m$ is transconductance
- $R_{DS}$ is output resistance
- $g_m = \frac{2I_D}{V_{GS}-V_{th}}$
- $V_{th}$ is threshold voltage

FETs vs BJTs for amplifier design in general...
- FETs more power efficient because they don’t take current as input
- BJTs more robust to power fluctuations and noise
- BJT’s capable of higher current gain and output voltage
- FET has higher input impedance (no current through gate)
  - In practice JFETS input impedance not as good as MOSFET why?
- Similar output impedance
- FETs to interact with digital circuits (i.e. digital control of a motor)
- BJTs have better high frequency response
**BJT Inverter**

- Very basic amplifier – $R_D$ and FET parameter, and is negative of input
- Infinite input impedance (theoretically)
- Tends to have poor bandwidth in AC applications
- Common Source Amplifier
  - **Input goes to Gate, Drain is output**, Source is common

### NOTE DIFFERENT RESISTOR VALUES!

<table>
<thead>
<tr>
<th></th>
<th>Formula</th>
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</thead>
<tbody>
<tr>
<td><strong>Current gain</strong></td>
<td>$i_{out}/i_{in} = \infty$</td>
</tr>
<tr>
<td><strong>Voltage gain</strong></td>
<td>$v_{out}/v_{in} = -g_mR_D$</td>
</tr>
<tr>
<td><strong>Input impedance</strong></td>
<td>$v_{in}/i_{in} = \infty$</td>
</tr>
<tr>
<td><strong>Output impedance</strong></td>
<td>$v_{out}/i_{out} = R_D$</td>
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FET Inverter with Source Resistor

- Improve stability/uniformity of the voltage gain at cost of lower gain
- \( g_m = \frac{2I_D}{V_{GS} - V_{th}} \) is a function of the inputs, so can vary with \( V_{GS} \)
- Common Source Amplifier
- We are not building this one today!

**Current gain**
\[ i_{out} / i_{in} = \infty \]

**Voltage gain**
\[ v_{out} / v_{in} = -\frac{g_mR_D}{1 + g_mR_S} \]

**Input impedance**
\[ v_{in} / i_{in} = \infty \]

**Output impedance**
\[ v_{out} / i_{out} = R_D \]
FET Voltage Follower

- Voltage gain is about 1, so it is used as a buffer and fixing impedance issues
- Common Drain Amplifier
  - Input goes to Gate, Source is output, Drain is common

<table>
<thead>
<tr>
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<th>Current gain</th>
<th>Voltage gain</th>
<th>Input impedance</th>
<th>Output impedance</th>
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<td>( \frac{i_{out}}{i_{in}} = \infty )</td>
<td>( \frac{v_{out}}{v_{in}} = -\frac{g_m R_S}{1 + g_m R_S} \approx 1 )</td>
<td>( \frac{v_{in}}{i_{in}} = \infty )</td>
<td>( \frac{v_{out}}{i_{out}} = \frac{R_S}{g_m R_S + 1} \approx \frac{1}{g_m} )</td>
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</table>
FET Current Follower

- Current gain is about 1, voltage amplified by function of FET and $R_D$
- Tunable output impedance and finite input impedance
- Used as voltage amplifier for high frequency applications
- Common Gate Amplifier
  - **Input goes to Source, Drain is output**, Gate is common

### Circuit Diagram

![Circuit Diagram](diagram)

### Equations

<table>
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<th>Equation</th>
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<td>Current gain</td>
<td>$i_{out}/i_{in} = 1$</td>
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<tr>
<td>Voltage gain</td>
<td>$v_{out}/v_{in} = \frac{R_D(g_m r_{ds} + 1)}{r_{ds} + R_D} \approx g_m R_D$</td>
</tr>
<tr>
<td>Input impedance</td>
<td>$v_{in}/i_{in} = \frac{R_D + r_{ds}}{g_m r_{ds} + 1} \approx \frac{1}{g_m}$</td>
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<tr>
<td>Output impedance</td>
<td>$v_{out}/i_{out} = R_D(g_m r_{ds} + 1) + r_{ds}$</td>
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Parameter Procedures

- For IV curve of FET use no resistor
- FET_IV.vi – set $V_{DS}$ to from 0V to 10 V at steps of .5V
  - Set $V_{GS}$ start to -3V, steps of 0.5V and 7 steps
- Don’t worry about other FET parameters
Amplifier Procedures

• Note different resistor values from instruction pdf!
• Tranchar.vi uses 2 source meters and power source for $V_{DD}=10V$
• For Invertor, set start $V=-4$, final $V=3$, step $=0.5V$
• Change the start or end to get a good view of the linear region. Calculate the gain from the slope.
• Set the function generator offset to the input voltage in the middle of the slope
  • Slowly increase the amplitude until clipping occurs at top and bottom
  • This should occur near where the function becomes nonlinear
  • You may need to adjust offset if only clipping one side
  • Recall that Function Generator may supply twice the voltage you expect!

![XY Graph](image_url)
Amplifier Procedures

- You can select XY graph by first hitting main/delayed then button below screen for XY
- XY graph should look like transchar graph.
- Remove sync for XY graph

- You can’t scopegrab XY graph, so it isn’t needed in report, but do this at least once
- For V. Follower tranchar, set start V=-4, final V=10, step =0.5V
- For C. Follower tranchar, set start V=-6, final V=5, step =0.5V