DEFECTS MODELING AND YIELD FORECASTING IN SEMICONDUCTOR MANUFACTURING

Abstract:
This project was completed during my one-year visit to IBM Research Center. We built a stochastic model reflecting the cause-and-effect connection between observed defects on manufactured chips and the chip failures. Many factors such as defect type, size, frequency, location play the role of covariates for the yield prediction. Estimation of a very large number of parameters is further complicated by a substantial portion of uninspected layers, unclassified defects, and other "surprises". Thus, advanced model calibration techniques are proposed. Results of this analysis are used for evaluating kill ratios, identifying the most dangerous cases, forecasting the yield, and designing optimal yield-enhancement strategies.

Besides this, it is a talk on how messy and dirty the data can be, and how complex the problems can become in real industrial setting.

Date: Tuesday, September 14, 2004
Time: 2:00 PM
Coffee will be served in ECSN 3.106 at 1:30 p.m.
Room: MP 2.214

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NOTE: Please contact Lorre Antoine at lantoine@utdallas.edu or (972)883-2161 or by FAX at (972)883-6622 for up-to-date seminar information if you want to receive e-mail notices.