Homework 1 Solutions

1. Admittance-Y Matrix for two-port network

\[ y_{11} = \left. \frac{i_1}{v_1} \right|_{v_2=0} = \frac{1}{R_i} \text{ (with the output short-circuited)} \]

\[ y_{12} = \left. \frac{i_1}{v_2} \right|_{i_1=0} = R_G \text{ (Reverse Transconductance)} \]

\[ y_{21} = \left. \frac{i_2}{v_1} \right|_{v_2=0} = G_m \text{ (Forward Transconductance)} \]

\[ y_{11} = \left. \frac{i_2}{v_2} \right|_{i_1=0} = \frac{1}{R_o} \text{ (with the input short-circuited)} \]

So voltage gain is,

\[ a_v = \left. \frac{v_2}{v_1} \right|_{i_2=0} = -\frac{y_{21}v_1}{v_1} / \frac{y_{22}}{v_2} = -\frac{y_{21}}{y_{22}} = -G_mR_o \]

2. Impedance-Z Matrix for two-port network
\begin{align*}
\begin{cases}
  v_1 = z_{11}i_1 + z_{12}i_2 \\
  v_2 = z_{21}i_1 + z_{22}i_2
\end{cases}

z_{11} &= \frac{v_1}{i_1} \bigg|_{i_2=0} \\

z_{12} &= \frac{v_1}{i_2} \bigg|_{i_1=0} \\

z_{21} &= \frac{v_2}{i_1} \bigg|_{i_2=0} \\

z_{22} &= \frac{v_2}{i_2} \bigg|_{i_1=0}
\end{align*}

Input resistance is

\[ R_i = \frac{v_1}{i_1} \bigg|_{i_2=0} = z_{11} \]

Forward transconductance is,

\[ G_m = \frac{i_2}{v_1} \bigg|_{i_1=0} = \frac{i_2}{z_{11}i_1 + z_{12}i_2} = \frac{i_2}{z_{11}(-z_{22}i_2 / z_{21}) + z_{12}i_2} = \frac{z_{21}}{z_{12}z_{21} - z_{11}z_{22}} \]

Output impedance is,
\[ R_o = \left. \frac{v_2}{i_2} \right|_{v_1=0} = \frac{z_{21}i_1 + z_{22}i_2}{i_2} = \frac{z_{21}(-z_{12}i_2 / z_{11}) + z_{22}i_2}{i_2} = \frac{-z_{12}z_{21} - z_{11}z_{22}}{z_{11}} \]

Voltage gain is,

\[ a_v = \left. \frac{v_2}{v_1} \right|_{i_2=0} = \frac{z_{21}}{z_{11}} = -G_m R_o \]

3. I-V curves of NMOS and PMOS transistors

NMOS schematic:

Id versus Vds (0-2.5V) under different Vgs(0-2.5V):
Id versus Vgs (0-2.5V) when Vds=2.5:

DC Response

\[ V_{gs} = \{0\}, \{0.5\}, \{1\}, \{1.5\}, \{2\}, \{2.5\} \text{V} \]

Vgs = "0"/M1/D, Vgs = "0.5"/M1/D, Vgs = "1"/M1/D, Vgs = "1.5"/M1/D, Vgs = "2"/M1/D, Vgs = "2.5"/M1/D

I vs Vgs (0-2.5V) when Vds=2.5:

DC Response

I (mA)

Vgs (V)

0.0 0.5 1.0 1.5 2.0 2.5

0 100 200 300 400 500 600
PMOS schematic:

Id versus Vsd (0-2.5V) under different Vsg(0-2.5V):

[Graph showing DC Response with different Vsg values]

Id versus Vsg (0-2.5V) when Vsd=2.5: