Switched-Capacitor Sample-and-Hold (S/H)

Overall Objective
This is the first of the three project assignments of this semester. The overall goal of this semester is to design a 100-MS/s, 12-b successive-approximation-register (SAR) analog-to-digital converter (ADC). At the end of the semester, you will have a design in 0.25-µm CMOS (with a 2.5-V VDD) that burns as low power as possible while meeting all the design goals.

Phase-I Objective
In this phase, you need to design a clock-bootstrapped bottom-plate sample-and-hold amplifier (SHA) as shown in the lecture. The tracking time is 2 ns, the holding time is 7 ns, and the non-overlapping time is 1 ns. This will give you a 100-MS/s sample rate. You will need to design everything at transistor level except the operational amplifier, which you may use an ideal VCVS as the model in your simulation. You need to evaluate your S/H performance in the inverting SHA configuration. You need to achieve as high linearity as possible.

Circuit Description
Refer to the lecture slides for the schematics of the inverting SHA. Set the capacitors to 2 pF each ($C_S = C_H = 2$ pF). The closed-loop gain should be very close to $-1\times$. Your maximum input and output swing should be 1.5 V, peak-to-peak. The circuit tracks the input in $\Phi_1$ and holds the sampled value in $\Phi_2$. To improve the S/H performance, you may want to bootstrap ALL switches in your design. Try to start from a sub-circuit of a single bootstrapped NMOS switch and instantiate your sub-circuit everywhere you need a switch in your design (you can size them with the M factor).

You may use an ideal VCVS to model the op-amp. If HSPICE complains for a small time step, try an internal RC circuit to limit the op-amp closed-loop bandwidth.

Use bottom-plate sampling to improve the linearity of the S/H circuit. An early phase is required in this scheme. You need to design a two-phase non-overlapping clock generator. Decide the optimal lead time of the early phase for your circuit. For the summing-node switch, you may choose either a three-switch configuration with a large differential switch plus two small single-ended switches with a proper summing-node common mode around VDD/2, or you can choose simply two single-ended switches. In either case, decide how to bootstrap these switches.

Design/Simulation Tasks
The most time-consuming part of your simulation is likely to be the transient. After you are done with the sizing of your circuit, apply a full-scale (1.5-Vpp) differential sine wave, say, around 10 MHz, to your SHA and watch its output waveform for a long period of time. Does the output resemble a sampled-and-held sine wave? If so, capture the SHA output at the end of $\Phi_2$ and perform an FFT on the discrete-time sample sequence. Try 64 samples to begin with. If you are not satisfied with the results, increase the number of samples to 256 (this will prolong your transient
simulation). Record the SNDR, SFDR, THD, dominant harmonics, etc. Repeat the simulation for ~25-MHz, ~50-MHz, and ~100-MHz inputs. Plot the SNDR, SFDR, and THD as a function of the input frequency.

Notes on Simulation and Results:
1. Robustness: repeat your simulation for VDD varying ±15% and temperatures at 0°C and 75°C. Document all FOUR results of your simulation in addition to the nominal case (2.5 V, 25°C).
2. Annotate your plots and draw lines/bounding boxes indicating target specs clearly.

Report Guideline
Write a concise report, not exceeding 5 pages for this phase of the project. Explain your design choices and demonstrate how your design meets all requirements. Please typewrite your report with simulation results/figures embedded/attached.