University of Texas at Dallas

Department of Electrical Engineering

EEDG 6306 - Application Specific Integrated Circuit Design

Homework #5

Due on Midnight 12:00, September 28th, 2016

Submission for Homework #5:

(1)Homework Report (2) Output file for HW5.in

Write a VHDL/Verilog code to implement the HW#4 algorithm.

(1. 1) Input file is provided on my webpage utdallas.edu/~zxb107020

(1.2) You may test your code's output by HW4 input set

(1.3) The filter's order N=256. Assume x(0-kmax)=···¬=x(-2)=x(-1)=0. **Your input start from X(0).**

(1.4) Computation should be done by addition and shift operations (Multiplication is not allowed). At each system clock cycle you can only execute one operation (shift or add).

(1.5) Your testbench should generate necessary signals to drive the computation as well as receive the output from the code. The final output should be printed to a file as HEX number (the same with HW3/HW4).

(1.6)You may hardcore the input data (rj/coeff) to your code for simplification purpose. In this HW, the 16 bits input data could be transmitted by parallel way to the code.

(1.7) The homework report should include the source code and waveforms to justify the function.